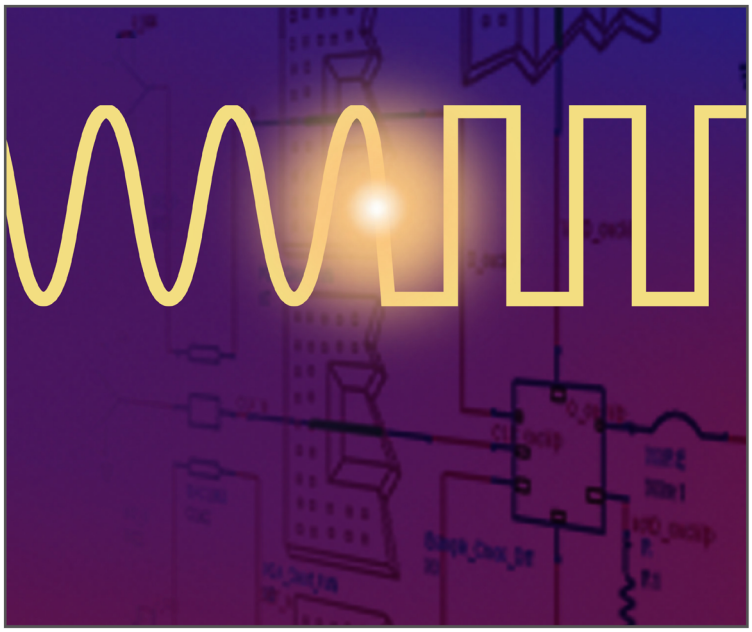
Keysight EEsof EDA

Advanced Design System

Circuit Design Cookbook 2.0



Advanced Design System

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KEYSIGHT TECHNOLOGIES

Table of Contents

Getting Started with ADS 2011

This tutorial provides getting started details to new users of ADS2011. ADS2011 organizes the design work in the form of workspaces. We need to create a new workspace to begin the design work.

ADS Licenses Used: Linear Simulation

Step 1 - Creating Workspace

1. Launch ADS2011 and from the main window select **File > New > Workspace**. Enter workspace name as desired, please note that the workspace name and path to the work-space location should not contain any spaces. Click **Next**.

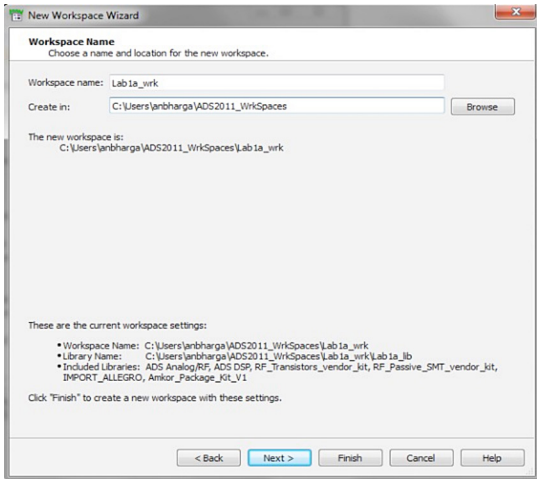


Figure 1.

2. Select the libraries to be included in the workspace. ADS natively provides the Analog/RF and DSP components library and it can be selected as needed in actual design work under the workspace. Component libraries provided in ADS can be added by clicking the link Add User Favorite Library/PDK (all vendor component libraries are provided in zipped format under:
<ADS_install_dir>/oalibs/componentLib/ folder)

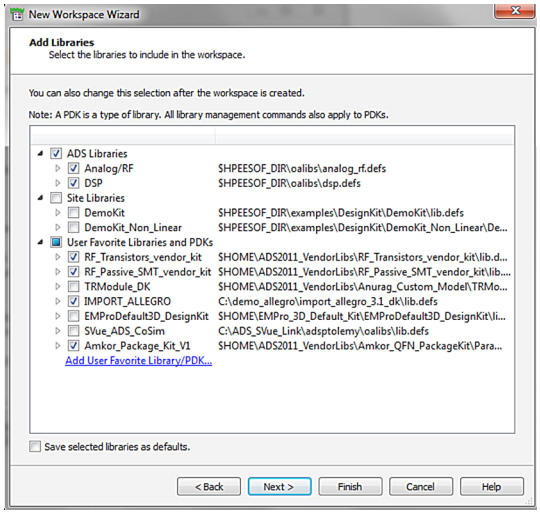


Figure 2.

3. Provide the library name under which you would like to organize the work. This library is not to be confused with component vendor or 3rd party libraries. This is a new way in which ADS2011 organizes the design schematics/layouts in a workspace and every workspace can contain multiple libraries in which we can organize our work consisting of multiple technologies e.g. GaAs, GaN, InP, SiGe etc. While we keep 1 library for each technology ADS2011 provides the capability to use these designs under a single main design to perform Multi-Technology designs. It may be noted that in ADS2011, schematic and layout units are also considered in different technologies and it is recommended not to mix the units which we use in design. i.e. mil, mm, um etc. Click **Next**.

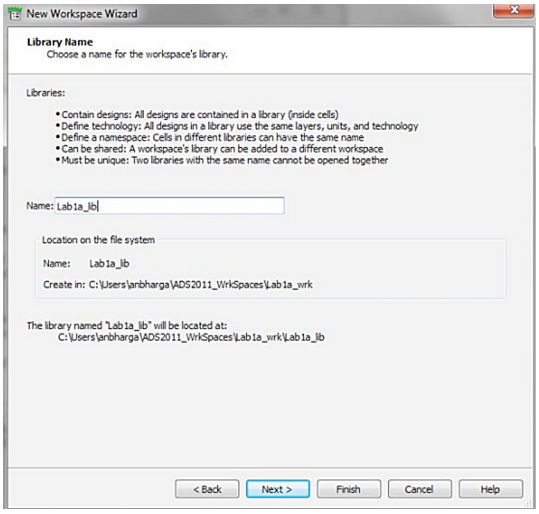


Figure 3.

4. Select the preferred units to be used during the design. In the present example, we select mil with 0.0001 mil layout resolution.

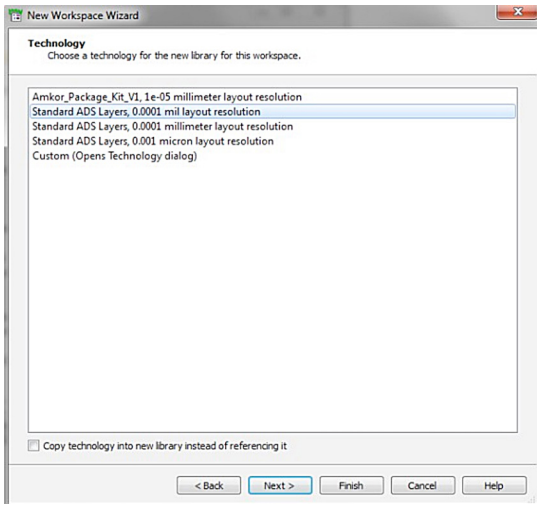


Figure 4.

5. Click **Next** and see the summary of the workspace and click **Finish** and a blank workspace as shown below will appear. We are ready to create our schematic or layout designs in the newly created workspace.

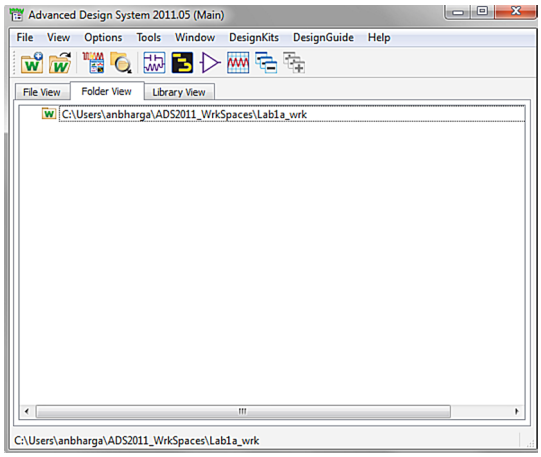


Figure 5.

Step 2 - Creating Schematic Design

Usually circuit design will start from schematic entry. To start the schematic design we can begin from **File >New >Schematic** or by clicking on the Schematic icon on the main window toolbar.

1. Enter the desired cell name (e.g. Discrete LPF) and select the Schematic Design Template as ads_templates: S_Params (for S-Parameter simulation). Selecting a template is an optional step but it is good feature to have because it saves the effort of setting up the design for simulation. Click **OK**.

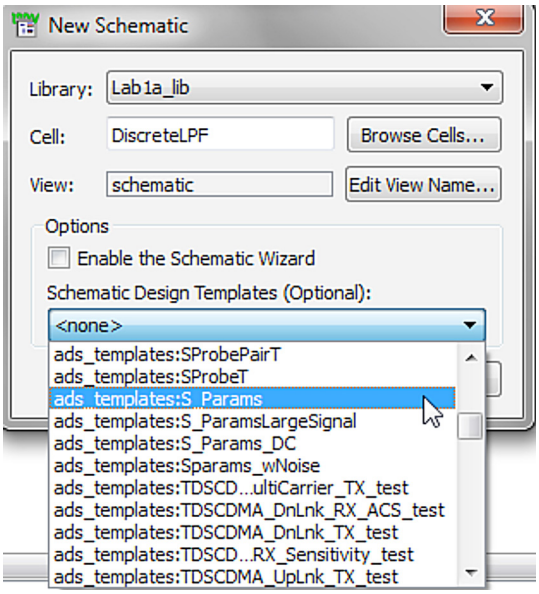


Figure 6.

2. A new schematic page with two 50-ohm terminations and an S-parameter controller placed on it with default frequency settings should be visible. If a template was not selected during new schematic creation then we can place required components for SP simulations by going to the appropriate Simulation category e.g. Simulation-S_Param, Simulation-HB etc.

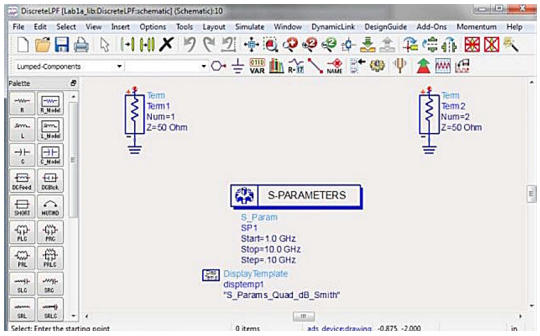


Figure 7.

3. Now let's start creating a circuit, go to **Lumped with Artwork** library as shown here, place **L_Pad** and **C_Pad** components on the schematic to form a Low Pass Filter Topology as shown in the Figure 8. L_Pad and C_Pad are normal inductor and capacitors but they also include footprint information and designers can enter desired width, spacing and length of the component as per the component that might be used for actual PCB design.

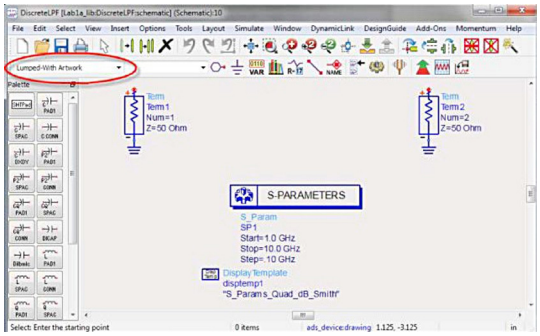


Figure 8.

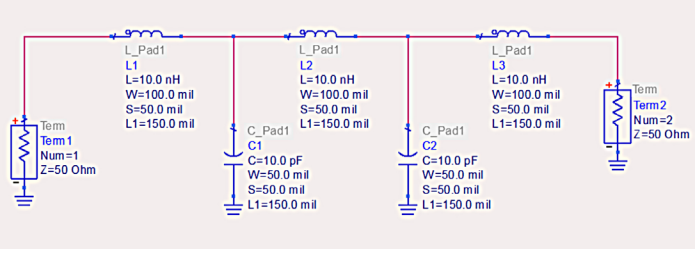


Figure 9.

4. Double-click the S-Parameter controller  and set the parameter as follows:
   - **Start** = 0.01 GHz
   - **Stop** = 1 GHz
   - **Num. of points** = 101 (step size will be automatically calculated) Click **OK**.

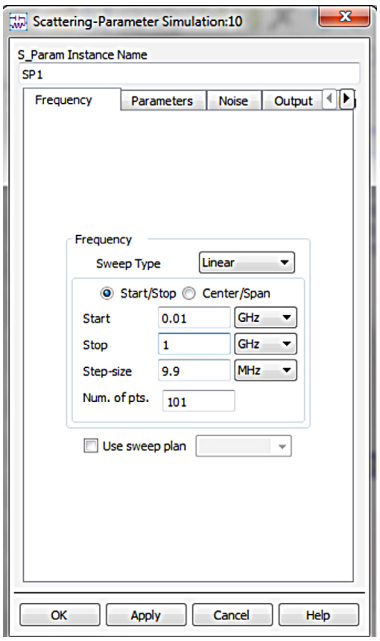


Figure 10.

5. Click the **Simulate** icon (or press F7) to start the simulation.
6. Once done, a data display shows the simulation results, as shown below.

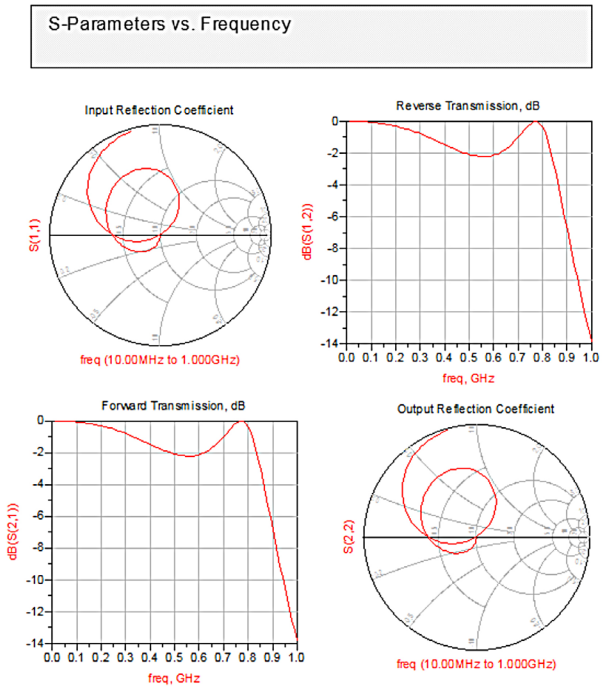


Figure 11.

7. Save the design to save all the work and inspect the main window to notice the schematic cell and data display (<filename>.dds).

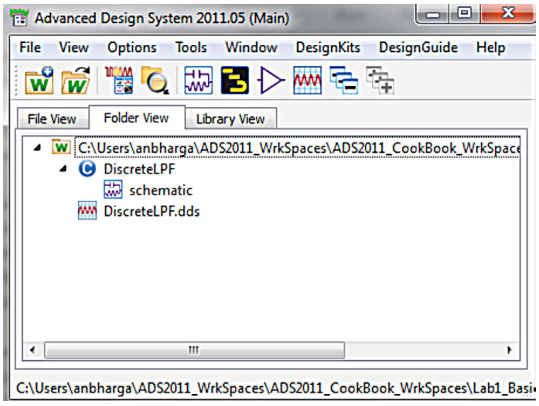


Figure 12.

Tuning and Optimization

ADS Licenses Used: Linear Simulation

It is often the case that our manually calculated values do not provide the most optimum performance, and we need to change the component values. This can be done in two ways: Tuning or Optimization.

What is Tuning?

Tuning is a way to change the component values and see the impact on circuit performance. This is a manual way of achieving the required performance from a circuit, which works well in certain cases.

What is Optimization?

Optimization is an automated procedure of achieving the circuit performance in which ADS can modify the circuit component values in order to meet the specific optimization goals. Please note that care should be taken while setting the goals to be achieved and it should be practically possible, otherwise it will not be possible to meet the goals. Also, the component values which are being optimized should be within the practical limits and this needs to be decided by designers considering the practical limitations.

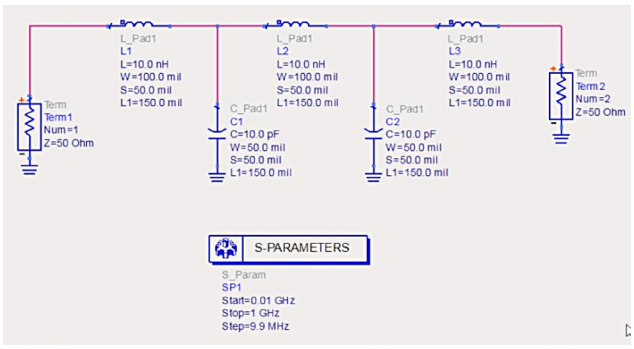


Figure 13.

Performing Tuning in ADS 2011

Let us take the LPF circuit example that we designed in the "Getting Started with ADS 2011" section and tune the component values in order to improve the circuit performance.

1. Open the LPF circuit as shown here. Delete the Display Template component and simulate.
2. In the data display, delete all the plots and insert a new rectangular plot.
3. Click the data display page and select S(1,1) and S(2,1) from the pop-up window and click **Add**>> and select units as dB when prompted.

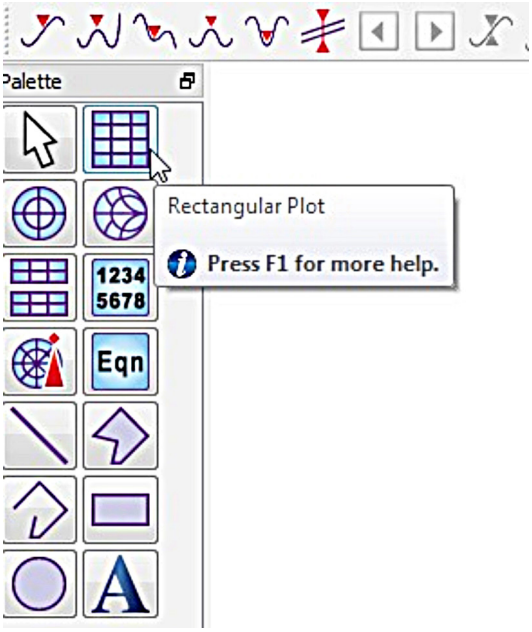


Figure 14.

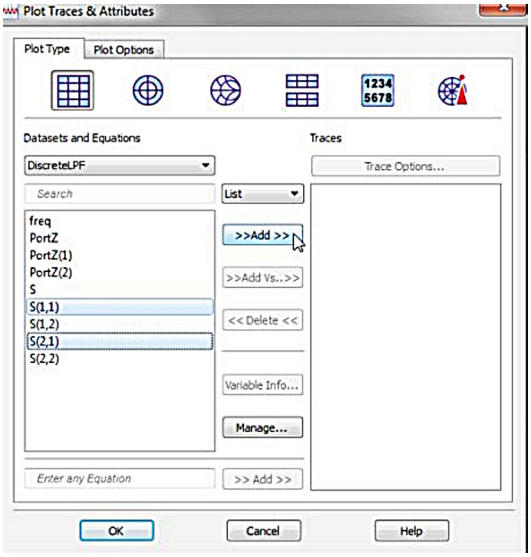


Figure 15.

4. Click **OK** to see the data display as shown below.

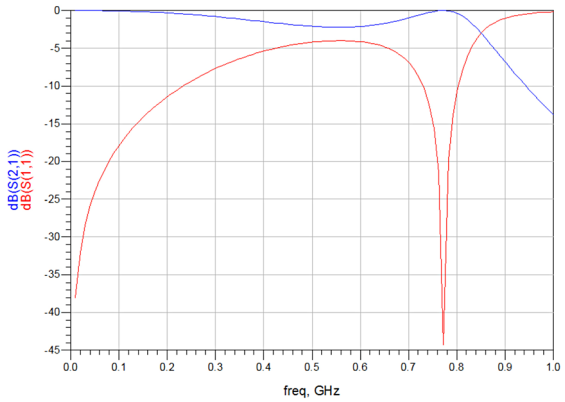


Figure 16.

5. Click the Tune Parameter icon on the schematic page
6. We need to make component values tunable in order to see their impact on circuit performance. Click inductance and capacitance **values of the components** in the LPF circuit and it will be added to the Tune wizard. If you click a component then you will get an option to select "L" or "C" etc. for tuning. Change the max values for all components to be 150 so that we have a decent range to tune the component values.

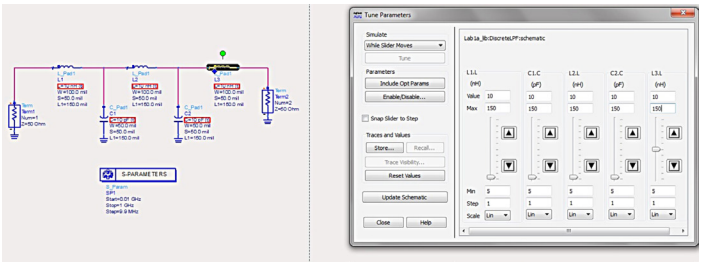


Figure 17.

7. Put the Tuning slider window and data display side by side and start to move the slider of component values and see the corresponding graph changing with the component values.

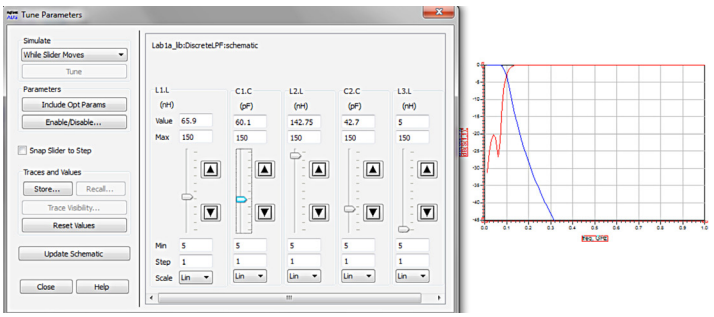


Figure 18.

Please note there are many other features of the Tuning wizard:

a. We can store temporary tuning states by clicking the Store icon so that we can save intermediate tuning conditions and revert back to any of the saved states by clicking the Recall button. These states will vanish once we close the wizard. Each saved state will result in a frozen trace in the graph window.
b. We can select "Snap Slider to Step" so that the slider changes in finite step size as mentioned in the Step field below the sliders.
c. Parameter values can be swept in Linear or Log format.
d. We can Enable/Disable a parameter to tune by clicking on Enable/Disable button.
e. If we have stored a lot of intermediate states, we can turn on/off a few graphs for better visibility.

8. Once we have achieved the desired or best possible results, we can click the **Update Schematic** button to update these tuning values on the design schematic. If you accidentally click Close, the pop up window will appear checking whether you would like to update your Schematic or not.
9. Click the Close button once you are done with tuning and observe the component values in the schematic and data display window for the tuned response.

Performing Optimization in ADS 2011

Let us now see how optimization can be performed on this LPF circuit to achieve the desired performance without us needing to do manual work.

Optimization in ADS is a 3 step process:

1. Setting up Optimization Goals
2. Placing Optimization Controller and select type of optimizer and number of iterations
3. Make component values optimization ready

Let's make a copy of the tuning schematic cell so that we can perform optimization on the same and also compare the responses of our manually tuned schematic and ADS optimized schematic.

1. Go to the Main Window and right-click the Cell to be copied and select "**Copy Cell**".

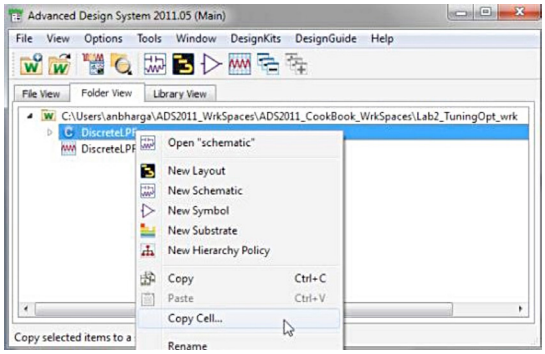


Figure 19.

2. A new pop window will appear and we can provide a new name for this copied cell, let's call it DiscreteLPF_Opt. Please note that if the cell that is being copied is hierarchal, then we should use the option "Include Hierarchy...", and if our workspace has folders, then we can copy this into the specific folder by clicking on "Choose Folder". Click OK after you are done with the actions mentioned above.

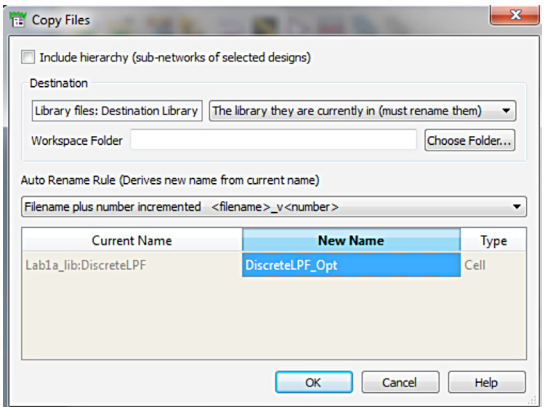


Figure 20.

3. Come back to the Main Window and observe that the cell is now copied and appears in the list with the new name as we provided during the copy process.

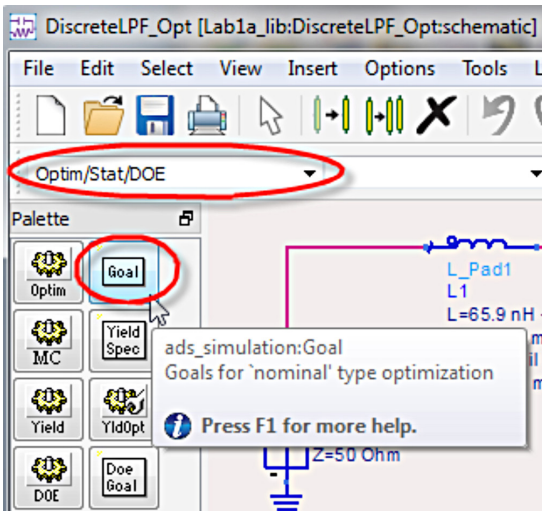


Figure 21.

4. Open the schematic view of this newly copied cell.

Setting Optimization Goals

1. Go to **Opt/Stat/DOE library palette** and place the **Goal** component on the Schematic as shown here.

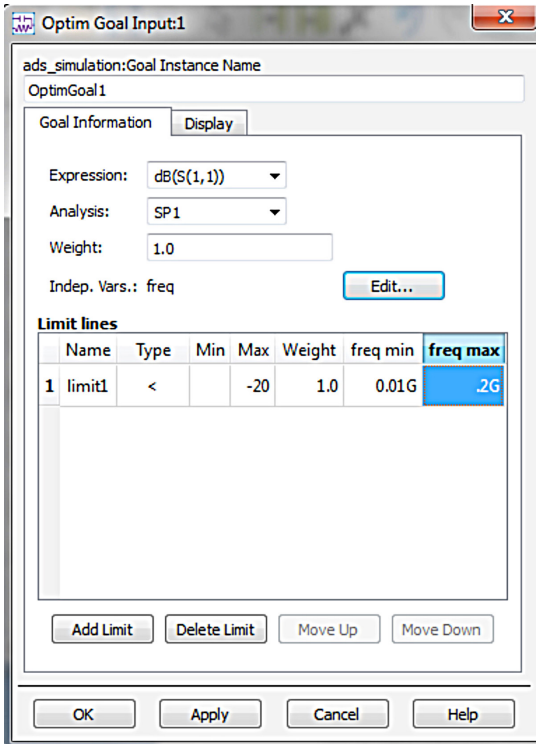


Figure 22.

2. Double-click the **Goal** component and enter parameters as follows:

   a. Expression = dB(S(1,1)) (same as what is available on the Y-axis of the graph).
   b. Analysis = SP1 (name of the S-Parameter controller available in our schematic).
   c. Click **Edit** in front of **Independent Var** and click **Add Variable** in the pop up window and enter **freq** as the variable name. ***freq*** *is the keyword for frequency which is our X-axis of the graph over which we will define this optimization goal.*
   d. Select **Limits->Type** as less than **(<)** and enter **-20**, this is to set dB(S(1,1)) to be better than -20 (dB is already defined in the S(1,1) definition, hence we don't need to define it again with -20).
   e. Enter freq min as 0.01G (which is the start frequency as we set in the S-Parameter controller), Enter freq max as 0.2G (max freq. up to which we would like to achieve this S11 goal).

3. Place another Goal and let's define dB(S(2,1)) i.e. Transmission response to be optimized.

   a. Repeat the same steps as done in defining the S(1,1) goal except for the fact that we can click Add limit to define stop band criteria as well.
   b. In the 1st limit (limit1) define the passband criteria as >-1 from freq min=0.01G to freq max=0.2G.
   c. In the 2nd limit (limit2) enter Type to be less than (<)-30 from freq min=0.4G & freq max=1G (max simulation frequency, should not be more than what is defined in the S–Parameter controller).
   d. We can add more limits as may be desired for the circuit response, e.g. for a typical band pass filter we will have three limits for S(2,1) and that is 1st for the lower stop band condition, 2nd for the upper stop band and 3rd for the main pass band.
   e. Once done, the S(2,1) goal window will look as shown here.

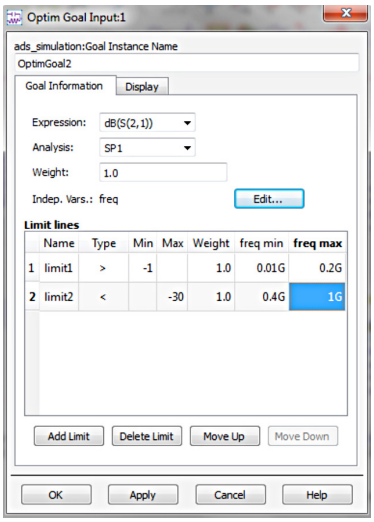


Figure 23.

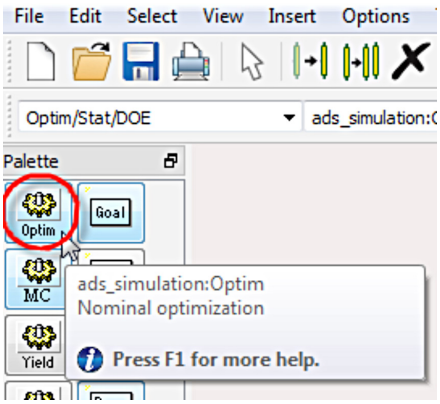


Figure 24.

Setting up Optimization Controller

a. Place Optimization controller on the schematic from **Opt/Stat/DOE** library, as shown above.
b. Double-click the Optimization controller and set parameters as below:
   a. Optimization Type = Gradient
   b. Number of Iterations = 2000
c. Go to the **Display** tab and select "Clear All" which will uncheck all options.
d. Select **Optim Type** and Max. Iteration options so that we will see only required options with this component in the schematic.
e. Click **OK** and the schematic as shown below should now be available.

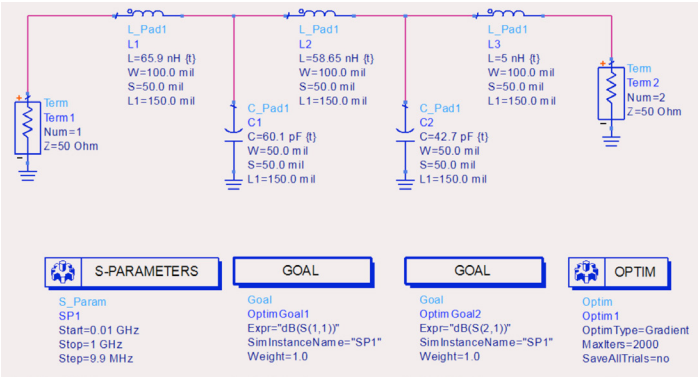


Figure 25.

Defining Component Values to be Optimization ready

The last step remaining for us to start the optimization is to set the component values to be optimization ready, which will then be changed by ADS during the optimization process.

1. Go to **Simulate->Simulation Variables Setup**.

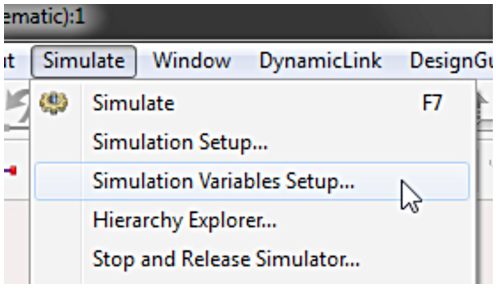


Figure 26.

2. Click the **Optimization Tab** in the variable setup window (this variable window is a single place where we define components to be tuned, optimized or to set their tolerances for Statistical analysis).

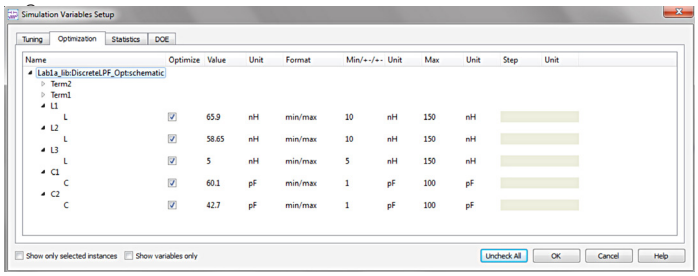


Figure 27.

Select all the "L" and "C" values to Optimize and set their min and max as per your own convenience (make sure that the value limits are realistic). We can also choose other Formats for defining a range of component values. Click **OK**.

Optimizing the Design

1. Click the Optimize button on the schematic toolbar (next to Tune icon).
2. The Optimization Cockpit window will open and we can see the circuit being optimized and component values being changed in order to meet the required goals that we have set on the schematic. Optimization takes 27 iterations (your case may be different as it depends on the response of your circuit from where you started optimization) to meet the goals as we desired and the optimization process will stop as soon as our goals are met, otherwise it will continue until we reach the max iteration limits. If we reach the max iteration limits before we meet the goals we should inspect the following:

   a. Whether Goals are realistic?
   b. Are we close to the components, min or max value (sliders will indicate that)?
   c. If we are reaching min and max limits of the component values, then we can click Edit variable and change the min/max if possible.
   d. We can increase the number of iterations by clicking on Edit Algorithm.
   e. We can modify the goal's setting by clicking on Edit goals.

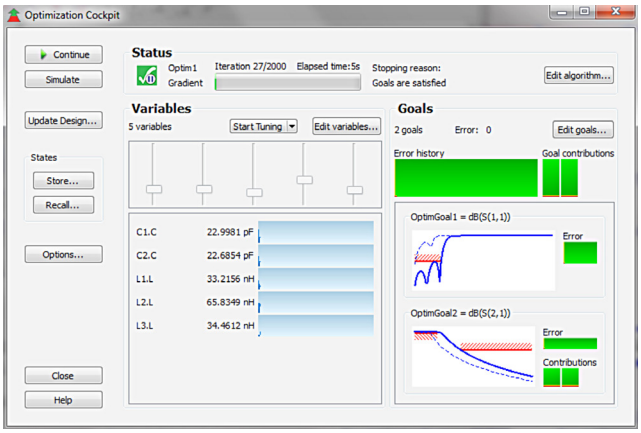


Figure 28.

There are many other exciting features in this optimization cockpit as mentioned earlier whereby we can pause the optimization, tune the values ourselves, Edit Goals on the fly, etc....try exploring these options at your convenience.

3. Click Close and select "Update the Design" option when prompted.
4. Plot the graph for S11 and S21 on the data display and check the circuit performance against our goals. We can place markers on these traces using either the Marker toolbar on data display or by going to the Marker menu.

Marker Toolbar:

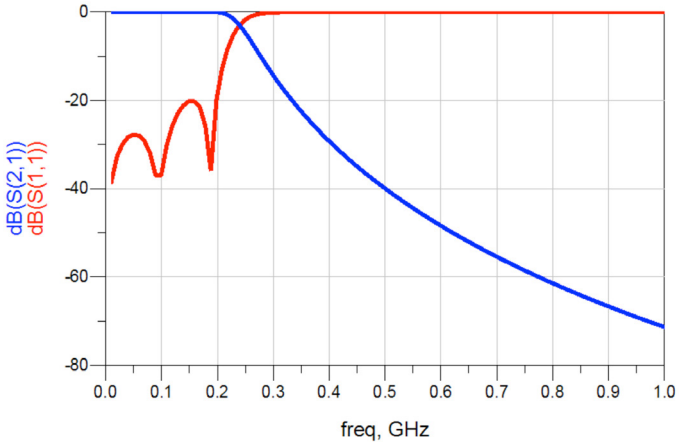


Figure 29.

5. Save all your work by going to **File > Save All** from the ADS Main Window.

Note:
The Optimization Goals setup, involving Optimization Goals and Controller, can be placed on a new blank schematic and then saved as our own template by going to **File->Save Design as Template.** This saves effort in setting up these things in future designs.

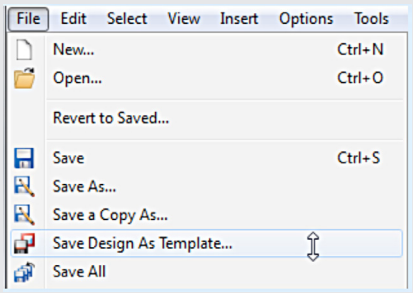


Figure 30.

This template can be inserted in any new design and under any workspace by going to **Insert >Template** and then selecting the template that we might have saved earlier.

Please note that optimization variables will be different in every design hence we need to redefine the component values to be optimization ready and set their limits.

Also, the goals/specifications may need to be altered as per the desired specs.

Important: Every single setup can be saved as a template for future use in ADS including the data display (which can be inserted in the data display page using **Insert >Template** option).

Harmonic Balance (HB) Simulation

ADS Licenses Used: Non-Linear Simulation (HB)

Harmonic Balance Basics

Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits and systems. It is well-suited for simulating analog RF and microwave problems, since these are most naturally handled in the frequency domain. You can analyze power amplifiers, frequency multipliers, mixers, and modulators etc., under large-signal sinusoidal drive.

Harmonic balance simulation enables the multi-tone simulation of circuits that exhibit inter-modulation frequency conversion. This includes frequency conversion between harmonics. Not only can the circuit itself produce harmonics, but each signal source (stimulus) can also produce harmonics or small-signal sidebands. The stimulus can consist of up to 12 non-harmonically related sources. The total number of frequencies in the system is limited only by such practical considerations as memory, swap space, and simulation speed.

The harmonic balance method is iterative. It is based on the assumption that for a given sinusoidal excitation there exist steady-state solutions that can be approximated to satisfactory accuracy by means of a finite Fourier series. Consequently, the circuit node voltages take on a set of amplitudes and phases for all frequency components. The currents flowing from nodes into linear elements, including all distributed elements, are calculated by means of a straightforward frequency-domain linear analysis. Currents from nodes into nonlinear elements are calculated in the time-domain. Generalized Fourier analysis is used to transform from the time-domain to the frequency-domain.

The Harmonic Balance solution is approximated by truncated Fourier series and this method is inherently incapable of representing transient behavior. The time-derivative can be computed exactly with boundary conditions, v(0)=v(t), automatically satisfied for all iterates.

The truncated Fourier approximation + N circuit equations results in a residual function that is minimized.

N x M nonlinear algebraic equations are solved for the Fourier coefficients using Newton's method and the inner linear problem is solved by:

- Direct method (Gaussian elimination) for small problems.
- Krylov-subspace method (e.g. GMRES) for larger problems.

Nonlinear devices (transistors, diodes, etc.) in Harmonic Balance are evaluated (sampled) in the time- domain and converted to frequency-domain via the FFT.

For a successful HB analysis:

1. *Add the Harmonic Balance* simulation component to the schematic and double-click to edit it.
   Fill in the fields under the Freq tab:
   - Enter at least one fundamental frequency and the number (order) of harmonics to be considered in the simulation.

     Make sure that frequency definitions are established for all of the fundamentals of interest in a design. For example, mixers should include definitions for RF and LO frequencies.

   - If more than one fundamental is entered, set the maximum mixing order. This limits the number of mixing products to be considered in the simulation. For more information on this parameter, see "Harmonics and Maximum Mixing Order" section under ADS HB Simulation documentation.

2. You can use previous simulation solutions to speed the simulation process. For more information, see "Reusing Simulation Solutions" under ADS documentation of Harmonic Balance.
3. You can perform budget calculations as part of the simulation. For information on budget analysis, see the chapter "Using Circuit Simulators for RF System Analysis" in the *Using Circuit Simulators* documentation.
4. You can perform small-signal analysis. Enable the *Small-signal* option and fill in the fields under the Small-Sig tab. For details, see Harmonic Balance for Mixers.
5. You can perform nonlinear noise analysis. Select the *Noise* tab, enable the *Nonlinear noise* option, and fill in the fields in the Noise (1) and Noise (2) dialog boxes.
6. If your design includes NoiseCon components, select the *Noise* tab, enable the *NoiseCons* option and fill in the fields.
7. If your design includes an OscPort component, enable Oscillator and fill in the fields under the Osc tab. Harmonic Balance for Oscillator Simulation focuses specifically on simulating oscillator designs.

Lab: HB Simulation Flow

1. Create a new workspace with name Lab2_HBSimulation_wrk.
2. Create a new Schematic Cell (name it as SystemAmp) and place the **Amp** model from **System- Amps and Mixers** library on the schematic.

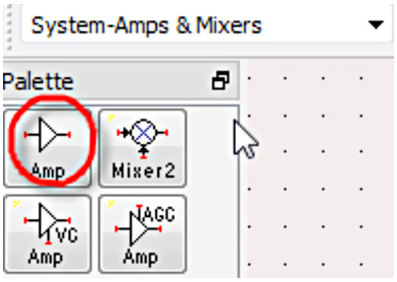


Figure 31.

3. Double-click the Amp component and set the Amplifier model parameters as below:
   - S21 = dbpolar(20,0)
   - S11 = dbpolar(-20,0)
   - S22 = dbpolar(-20,180)
   - S12 = dbpolar(-35,0)
   - TOI = 20
4. Place the P_1Tone source from the **Sources-Freq Domain** library and set its parameters as below;
   - P = polar(dbmtow(pin),0)
   - Freq = 5 GHz

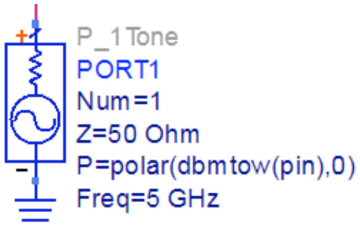


Figure 32.

dbmtow() is a function that converts the dBm power we enter in the source to watts for internal calculation purposes.

5. Place the **Term** component from the **Simulation-HB** palette library after the Amplifier and make connections as shown.
6. Click the **Wire Label** NAME icon, enter the name as **vout** and click the **Term** component's "+" pin as shown in the snapshot here.

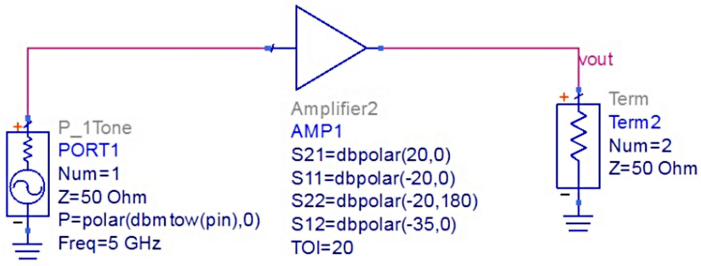


Figure 33.

7. Place the HB simulation controller from the Simulation-HB library palette and set Freq = 5GHz (same as defined in the 1-Tone source).
8. Click the **VAR** icon on the toolbar and define a new variable with a pin value of -20.
9. Once done, the schematic will look as shown below.

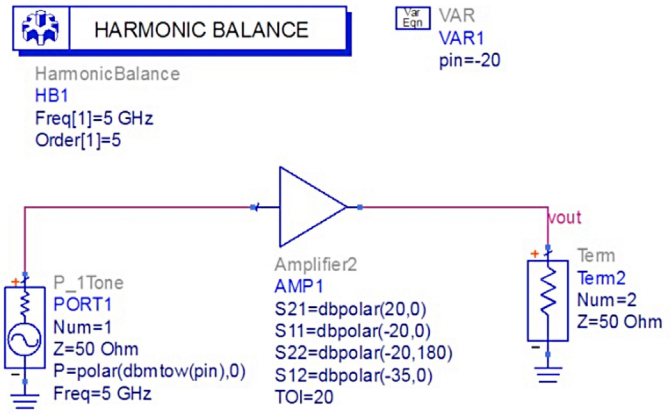


Figure 34.

10. Run the simulation and plot a graph in data display and select "vout" from the available list and select units as "Spectrum in dBm" and observe the data display as shown below:

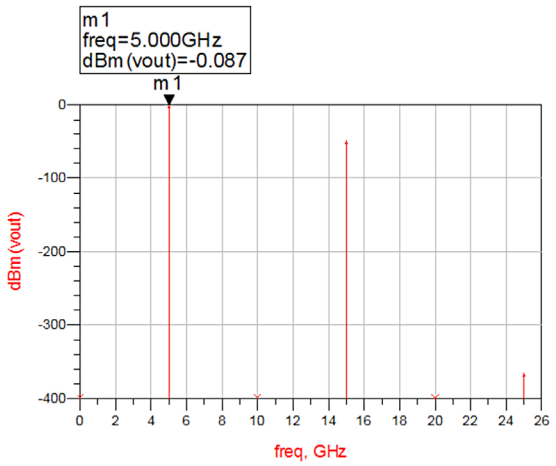


Figure 35.

Lab: Power Sweep Simulation

1. Make a copy of the cell, by right clicking on the existing cell and select Copy Cell.
2. Give it a new name, e.g. SystemAmp_PSweep.
3. Open the schematic of this copied cell and double click the HB Simulation controller.
4. Go to the Sweep Tab and enter:
   - **Parameter to Sweep = pin**
   - **Start = -30**
   - **Stop = 0**
   - **Step-size = 1**

These settings state that we will sweep pin (input power) from -30 dBm to 0 dBm in a step of 1 dBm.

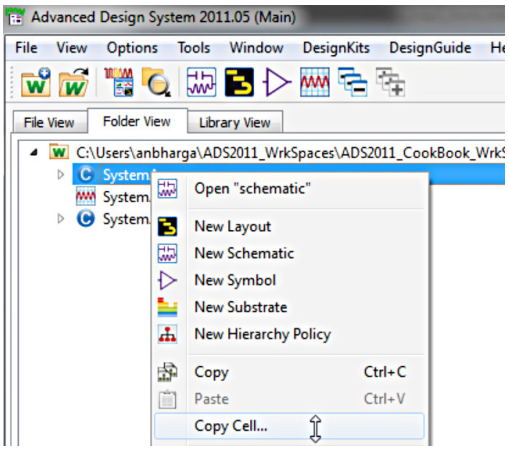


Figure 36.

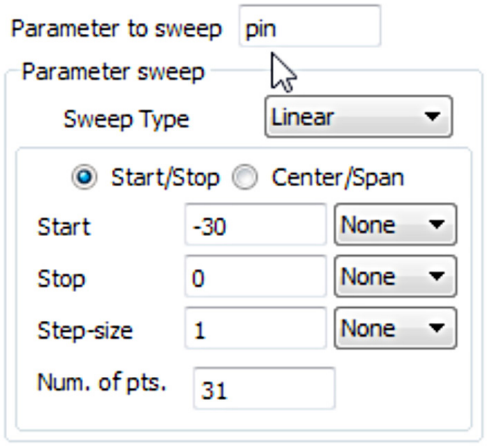


Figure 37.

5. Run the simulation and insert a new Rectangular plot and select “vout” to be plotted, select “Fundamental tone in dBm over all sweep values”. Observe the data display as shown here:

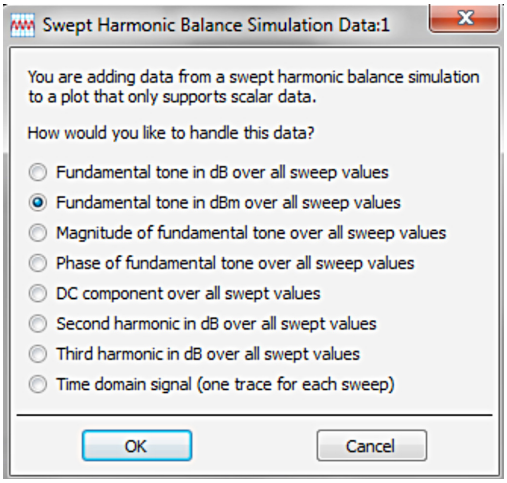


Figure 38.

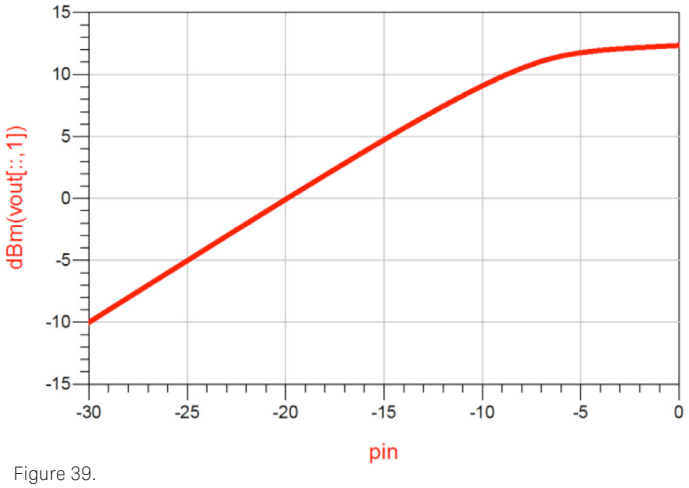


Figure 39.

6. Insert an **Eqn** on the data display and enter an equation for calculating the gain curve of the amplifier:
   - Gain = dBm(vout[::,1]) – pin
   - Insert a new rectangular plot and click the Datasets and Equations drop down menu, select **Equations**
   - Select **Gain** (or whatever name was given in equations)
   - Click **OK** to plot the Gain response as shown below

Eqn Gain=dBm(vout[::,1])-pin

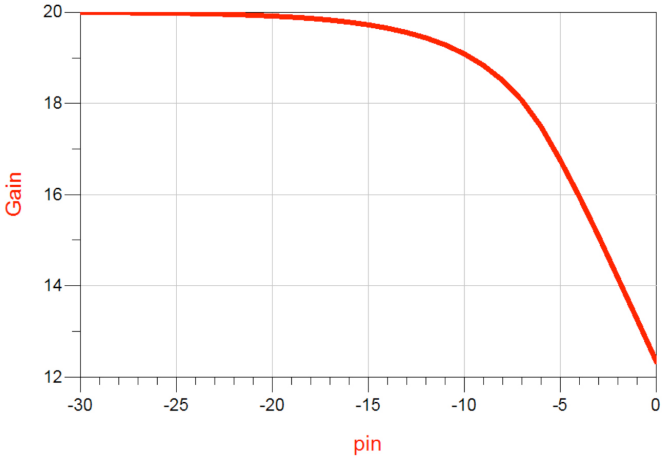


Figure 40.

Notes:

1. Take some time to think about Y-axis value dBm(vout[::,1]). Data available at "vout" is a 2-dimensional array, with the 1st argument being swept power (pin) and the 2nd argument being frequency tones (5 harmonics as selected in the HB controller i.e. Order=5).

2. In order to get more clarity on the array indexing, double-click the graph and select "**vout"** and click the **Variable Info** button to see details of the data available at the **"vout"** node, as shown here:

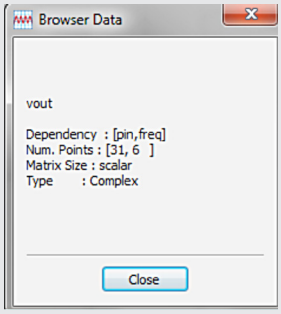


Figure 41.

3. Add "vout" on the graph like we did earlier and select the same option of adding a fundamental tone in dBm on all sweep values...

4. Now 2 traces should be visible on the graph, click the Y-axis label for one of the graphs and it will become editable, change the label to dBm(vout[::,3]) to see traces of the fundamental frequency and 3rd harmonic along with the fundamental.

5. Place a Line Marker to see values of the traces. Note the slope of the fundamental and 3rd harmonic (3 times higher than fundamental).

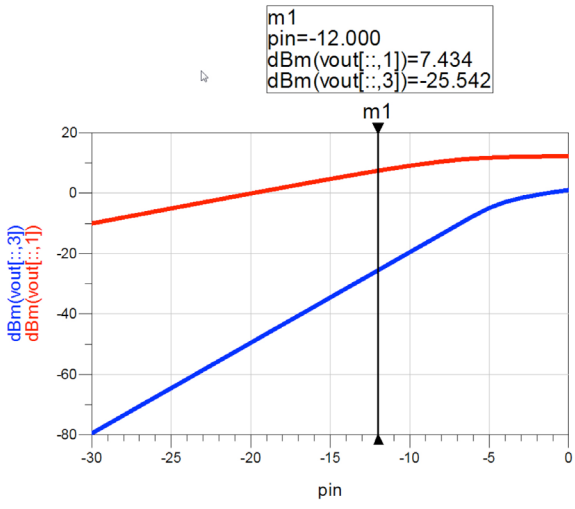


Figure 42.

Planar Electromagnetic (EM) Simulation in ADS

ADS Licenses Used: Linear Simulation, Momentum Simulation

Keysight ADS provides two key electromagnetic simulators integrated within its environment, making it convenient for the designers to perform EM simulations on their designs. Unlike circuit simulators, EM simulators are used on layout.

This chapter illustrates the flow that can be used to perform EM simulations as needed by designers using the ADS2011 (& beyond) release.

Case Study 1: Microstrip Bandpass Filter

Step 1 - Creating the Schematic Design for a BPF

Create a new workspace and select units as "mil". Create a new schematic cell and place components for a coupled line bandpass filter topology as shown below.

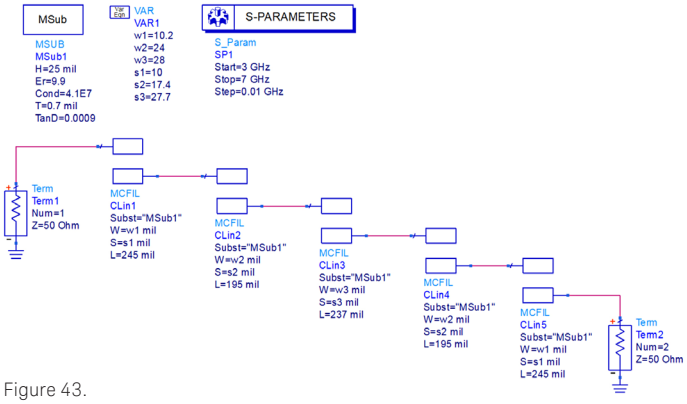


Figure 43.

In order to prepare this 5-section Coupled Line BPF, do the following:

1. Place MCFIL (Coupled Filter Section) from TLines-Microstrip library palette.
2. Place a VAR block and enter w1, w2, w3, s1, s2, s3 variables with values as shown here.

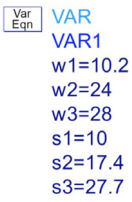


Figure 44.

Modify the values in MCFIL components to reflect these variable values for W– and S–parameters (please note that units are in mil)

3. Define lengths for MCFIL components as below:
   - 1st and 5th section: 245 mils
   - 2nd and 4th section: 195 mil
   - 3rd (center) section: 237 mil

4. Define a microstrip substrate(MSUB) with the following values:
   - H=25 mil (Height of the dielectric)
   - Er=9.9 (Relative Dielectric constant)
   - Cond=4.1E7 (Metal Conductivity, in this case it is set for Gold)
   - T=0.7 mil (Metal Thickness)
   - TanD=0.0009 (Loss Tangent)
5. Place two 50-ohm terminations (Term) components at the input and output from the Simulation- S_Param library palette
6. Place the SP controller from the Simulation-S_Param library palette and set its frequency as 3 GHz – 7 GHz with a step size of 0.01 GHz
7. Run the simulation and observe the results. It should be similar to the one shown below.

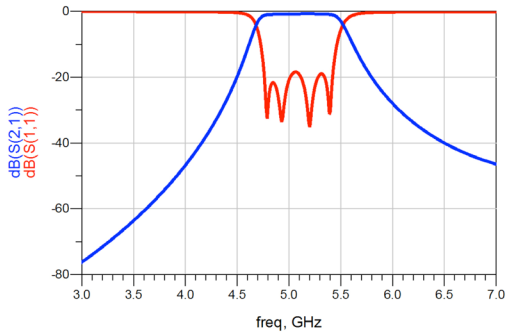


Figure 45.

Step 2 - Creating the Layout from Schematic

Create the layout from schematic by going to **Layout >Generate/ Update Layout**. Click **OK**.

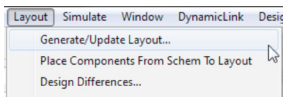


Figure 46.

Once done, layout as shown below should be available and layout view will be added in the view list under the cell name and same can be verified the ADS Main Window.

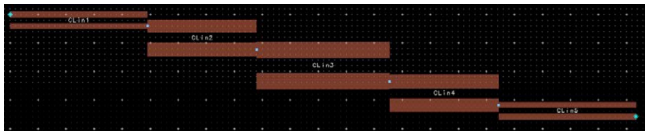


Figure 47.

Step 3 - Setup and run EM simulation

To run the EM simulation we need to setup the required things properly. Basic steps involved in running proper EM simulations are as below:

1. Connect the Pins in layout, which then will be defined as Ports in the EM setup window

Note:
We do not need to convert Pins to Ports where we don't need to see the results. This reduces the simulation dataset size).

2. Select the right simulator – Momentum (Method of Moments) or FEM (Finite Element Method)
3. Define the proper substrate definition
4. Define the simulation frequency plan
5. Define the conductor meshing properties
6. Create EM Model & symbol – This is an optional step and can be left out if it is not needed to run an EM-Circuit co-simulation i.e. to combine discrete components along with layout (this feature is explained in subsequent text)

Let us now begin the EM simulation setup as described above:

1. Connect the Pins at the input and output of the filter structure

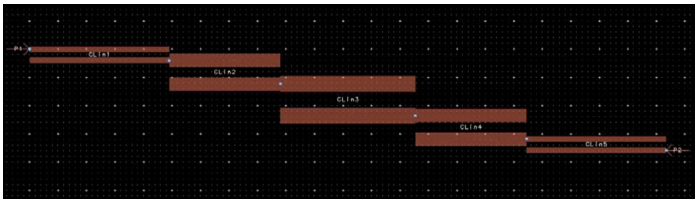


Figure 48.

2. Click the EM setup from the EM simulation toolbar on the layout page as shown below

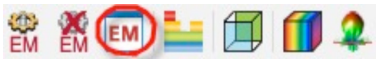


Figure 49.

   a. EM setup window as shown below appears and you can note the ⚠ indicating that there is something missing from the setup. Hovering the mouse over ⚠ the warning will complain about the substrate, because we haven't defined the substrate yet.

3.

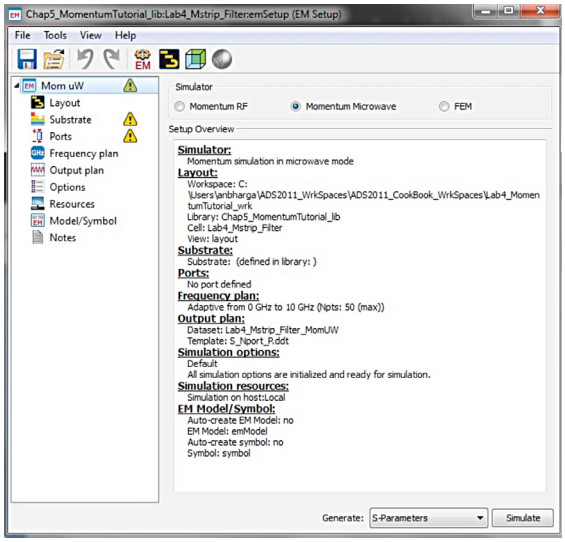


Figure 50.

   b. Click the **Substrate** option and click **New** and then click **OK** to accept the *25 mil* Alumina template and we can modify the properties of the same to suit our applications.

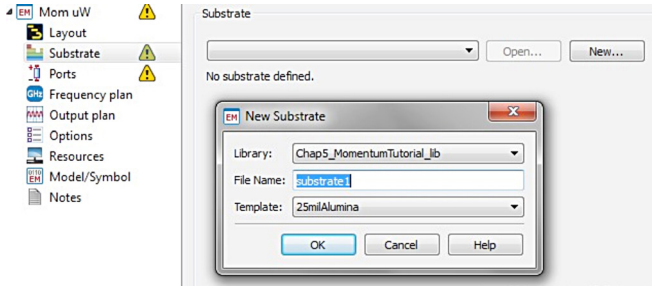


Figure 51.

c. Once we click **OK**, the substrate editor as shown below will be opened, click the Alumina dielectric and click the "...." button as indicated by the mouse cursor in the snapshot below:

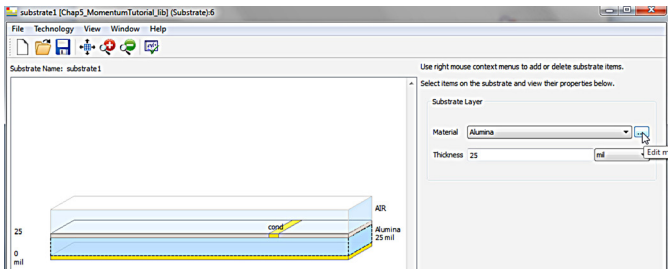


Figure 52.

d. In the pop window, modify the Alumina characteristic to have *Er=9.9* and *TanD=0.0009*, which is the same as we used in schematic design

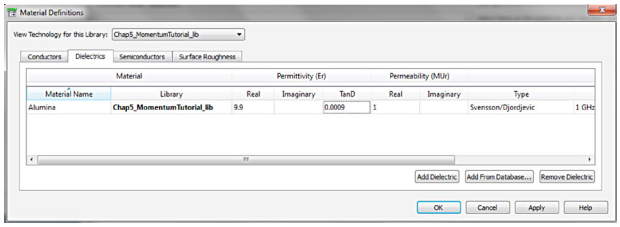


Figure 53.

e. Click the **Conductors** tab, go to "Add from Database" and select "Gold" from the list and click **OK**.

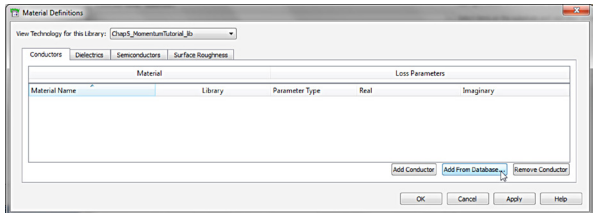


Figure 54.

f. Click **OK** once you are done defining the dielectric and conductor properties. From the main substrate definition window, click "cond" from the graphic window and select "Gold" from the Material list and define the thickness as *0.7 mil*.

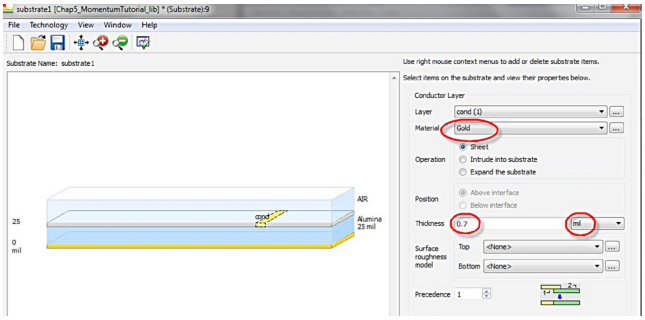


Figure 55.

Note:
"cond" is defined as a Sheet for Thick conductor. You can also select "Intrude into substrate" or "Expand the substrate". If it is defined as Sheet, then we need to use Edge Mesh as defined in point (5) later. Edge Mesh can be ignored if we defined the conductor as a Thick conductor.

g. Click Save and close the substrate editor window once the substrate is defined properly.

Note:
We can add more dielectric layers, Via etc. by right-clicking the graphics in the substrate editor window.

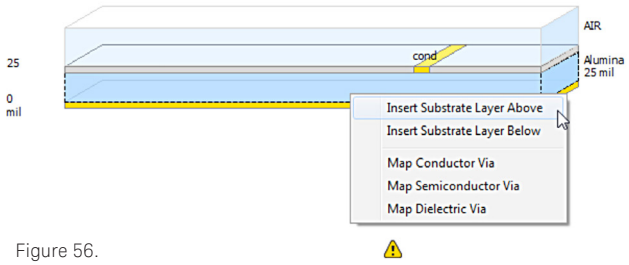


Figure 56.

h. Now the EM setup window should not have any ⚠ mark visible. If you still see it, try hovering the mouse over it to see what mistake was done while following the steps above.

4. Click **Ports** in the EM setup window to inspect that there are 2 ports defined (1 for each pin placed in layout) as shown below.

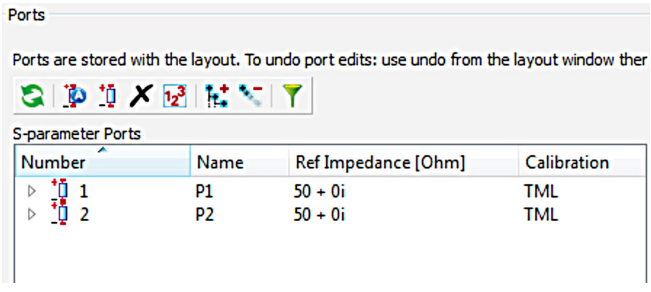


Figure 57.

5. Click the **Frequency Plan** and define the Sweep Type to be Adaptive, *Fstart=3 GHz*, *Fstop=7 GHz* and *Npts=101*.

6. Frequency Plan

	Type	Fstart	Fstop	Npts	Step	Enabled
1	Adaptive	3 GHz	7 GHz	101 (max)	-	☑

Figure 58.

Note:
- Adaptive is the preferred mode of sweep in EM simulation and not Linear as in the case of Schematic simulation.
- You can add more segments by clicking on the Add button.

7. Click **Options** and go to the **Mesh** tab and select Edge Mesh and leave other fields as default.

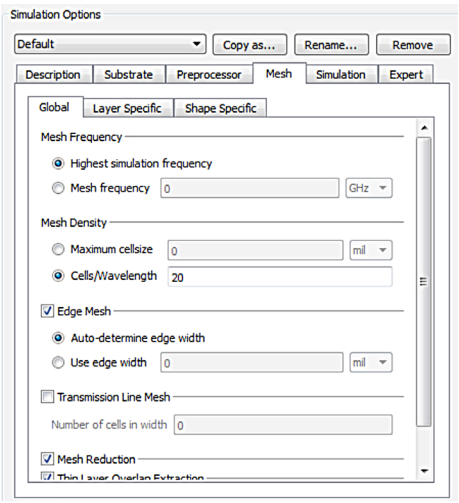


Figure 59.

8. Now we are done with the EM setup, click the **Save** button and click the **Simulate** button at the bottom right-hand side of the EM setup window.

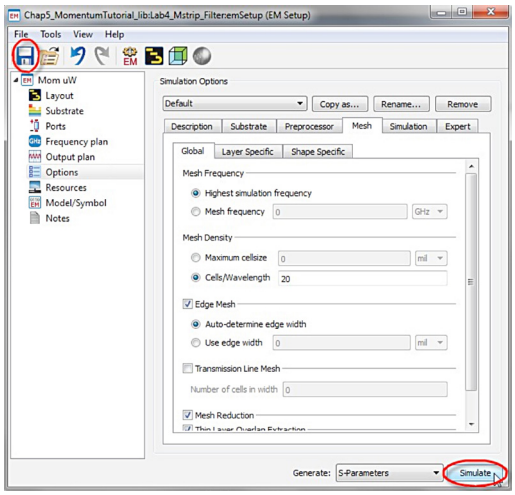


Figure 60.

9. This will pop-up the following 2 windows: **Job Manager** and **Momentum Simulation Status** window as illustrated:

   - **Job Manager** window: displays simulation job status. Its status turns to "Done" once simulation is finished.

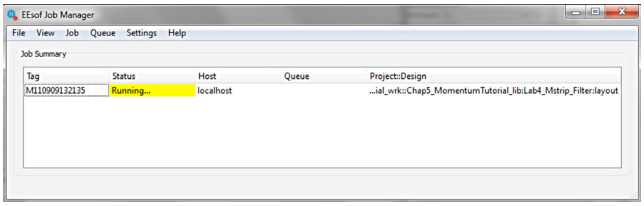


Figure 61.

   - **Momentum Simulation Status** window: displays simulation status. It shows the time when simulation is finished and displays frequency points to achieve the converged results for the sweep we performed e.g. 15 frequency points in the example simulation illustrated. This happened because we selected sweep type as Adaptive and it automatically stops once we have the converged results.

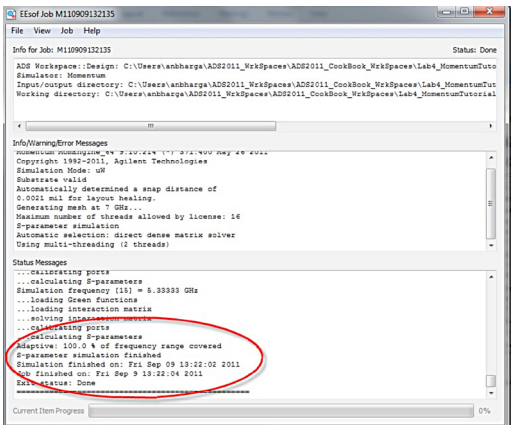


Figure 62.

10. The Momentum simulation data display will open automatically. Delete all the graphs and insert a new rectangular graph and select S(1,1) and S(2,1) to be plotted in dB scale (when prompted).

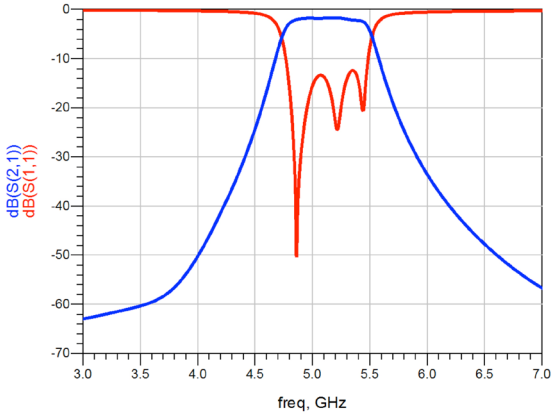


Figure 63.

Note:
When we perform Adaptive frequency sweep, ADS generates 2 dataset files; one for the points which are simulated (in our case: 15 freq points) and the other one with "_a" suffix indicating the adaptive rational polynomial fitted curve as illustrated. The dataset with "_a" suffix is recommended to be used for display purposes.

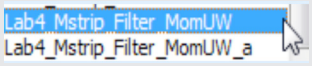


Figure 64.

Step 4 - Comparison of EM and Schematic Results

The last step is to compare the EM and schematic results. In order to see both the results on the same graph, double-click the Momentum graph and click the drop down list to locate the dataset for the circuit. It should have the same name as the cell name (e.g. Lab4_Mstrip_Filter). Select S(1,1) and S(2,1) in dB. Observe the response for both circuit simulation as well as Momentum simulation.

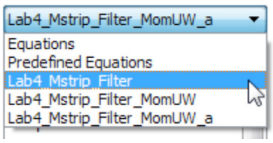


Figure 65.

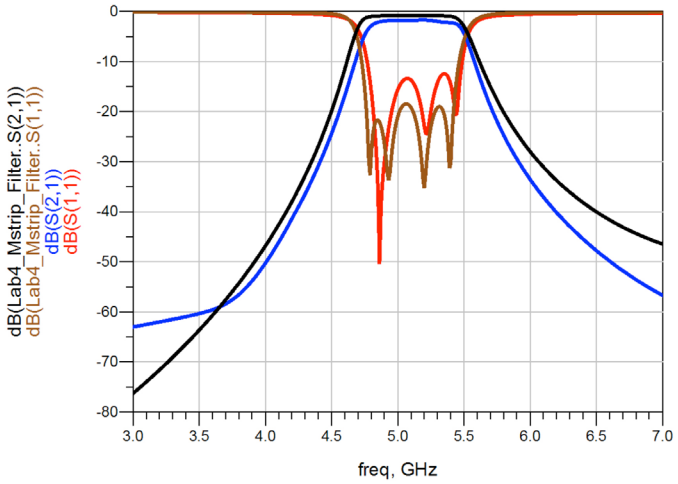


Figure 66.

Case Study 2: Design and Simulation of Patch Antenna

Theory

A microstrip antenna in its simplest configuration consists of a radiating patch on one side of a dielectric substrate, which has a ground plane on the other side. The patch conductors are usually made of copper or gold can be virtually assumed to be of any shape. However, conventional shapes are normally used to simplify analysis and performance prediction. The radiating elements and the feed lines are usually photo etched on the dielectric substrate. The basic configuration of a microstrip patch antenna is shown in the following illustration.

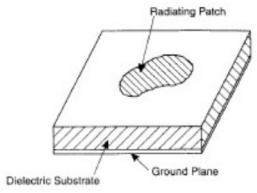


Figure 67.

The radiating patch may be square, rectangular, circular elliptical or any other configuration. Square, rectangular and circular shapes are the most common because of ease of analysis and fabrication. Some of the advantages of microstrip antennas compared to conventional microwave antennas are:

- Low weight, low volume
- Low fabrication cost
- Easy mass production
- Linear and circular polarization are possible with simple feeds
- Easily integrated with MIC
- Feed lines and matching networks can be fabricated simultaneously with antenna structures

Patch antennas find various applications from military to commercial, because of their ease of design and fabrication. Patch arrays are extensively used in phased array radar applications and in applications requiring high directivity and narrow beam width.

Objective

To design a Patch antenna at 2.4 GHz and simulate the performance using ADS 2011 (or later)

Step 1 - Calculating Patch Antenna Dimensions

Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the patch antenna. In the present case, we shall use the following Dielectric for design:

a. Height: 1.6 mm
b. Metal Thickness: 0.7 mil (1/2 oz. Copper)
c. ε_r: 4.6
d. TanD: 0.001
e. Conductivity: 5.8E7 S/m

11. Calculate the physical parameters of the patch antenna as shown in the geometry in the following illustration using the given formula.

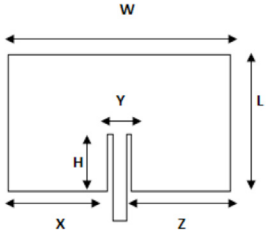


Figure 68.

The width and length of the radiating surface is given by,

$$W=L=\frac{c}{(2f\sqrt{\varepsilon_r})} = 29.2\text{mm}$$

where,

- Velocity of light c = 3 X 10^8 m/s^2
- Frequency, f = 2.4 GHz
- Relative Permittivity ε_r = 4.6

The depth of the feed line into the patch is given by:

H=0.822*L/2 = 12 mm

The other dimensions are,

- Y= W/5 = 5.8 mm
- X = Z = 2W/5 = 11.7 mm

Step 2 - Creating Patch Antenna Geometry

1. Create a new workspace, name it **Lab5_PatchAntenna_wrk**
2. Open the new layout cell and name it **Patch_Antenna**
3. Use **Insert ->Polygon** and use **Insert->Coordinate Entry** commands to enter (X,Y) coordinates to enter the required points to construct the Patch Antenna geometry as per our calculations:

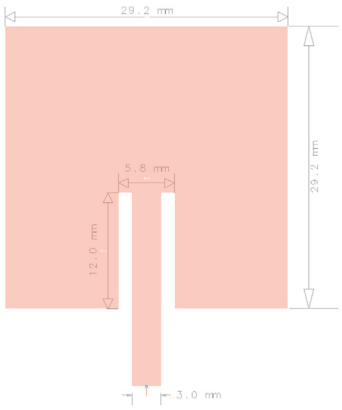


Figure 69.

Step 3 - Antenna Simulation

Connect a pin at the feed point of the antenna as shown below

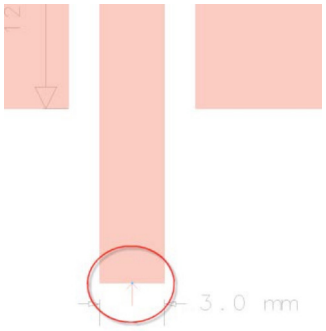


Figure 70.

4. Go to the EM setup window and click Substrate and click **New** to accept the 25 mil Alumina template. Define the substrate as below, modify the default substrate height, Er, TanD and conductor height and define it as Copper (select it from Add from Database list). Changing the name of the dielectric is optional as it has no bearing on the simulation.

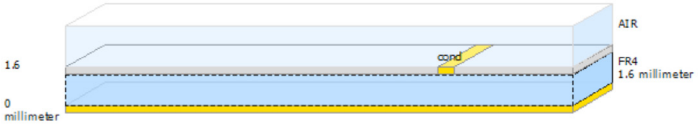


Figure 71.

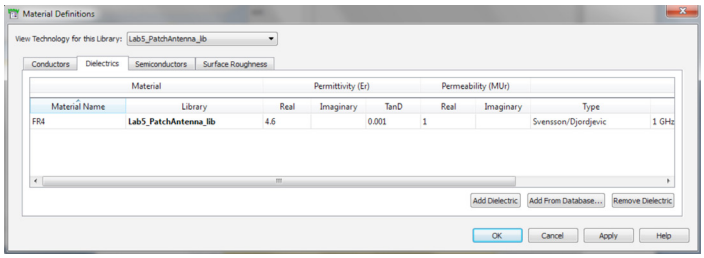


Figure 72.

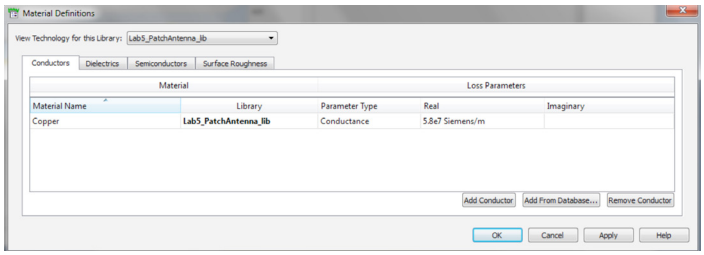


Figure 73.

5. Set the **Simulation Frequency range** as 2.1GHz – 2.7GHz (adaptive sweep) and Add a new Single Point of 2.4GHz as shown below

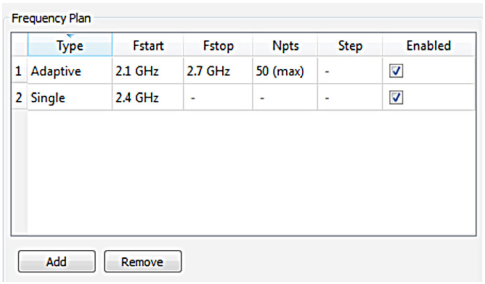


Figure 74.

6. Click **Simulate** and observe the simulation results in the data display

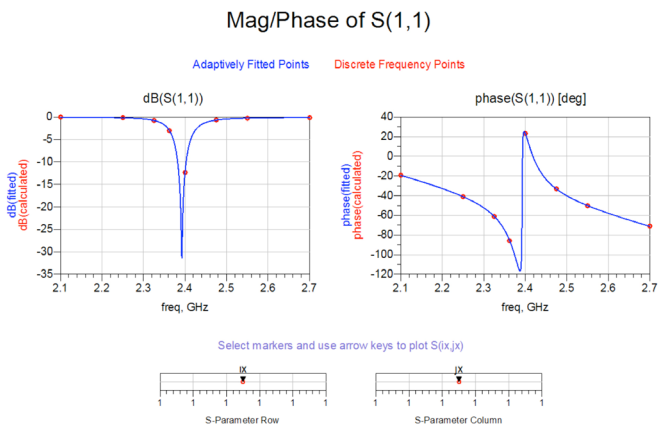


Figure 75.

Step 4 - Antenna Radiation Pattern

1. For the Far-Field Antenna Pattern, go to **EM > Post Processing > Far Field** and select the desired frequency (e.g. 2.4 GHz) and click **Compute**.

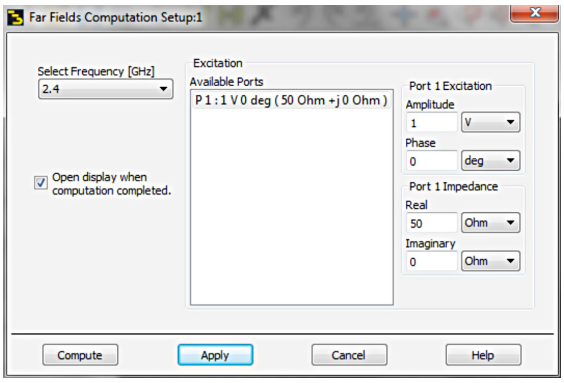


Figure 76.

2. Far field computation will be done and results will be displayed in the post processing window as shown below. We can use **Window >Tile** and then go to **Plot Properties** (from the bottom tabs) and then select **Far Field >Antenna Parameters** to see all the required data.

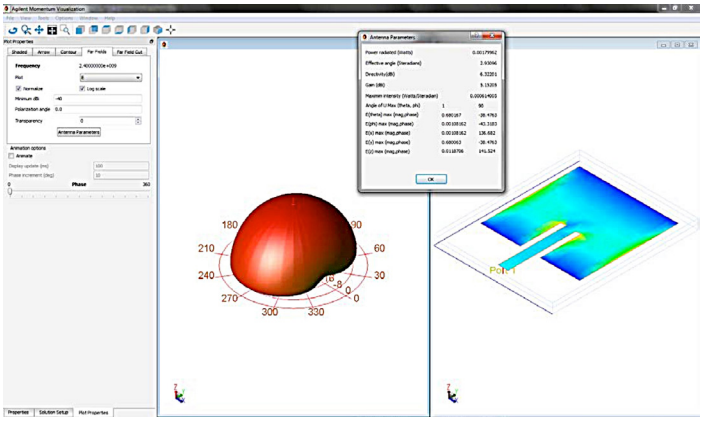


Figure 77.

3. Go to **Far Field Cut** tab and select the desired Phi and click **Display Cut in data display** button

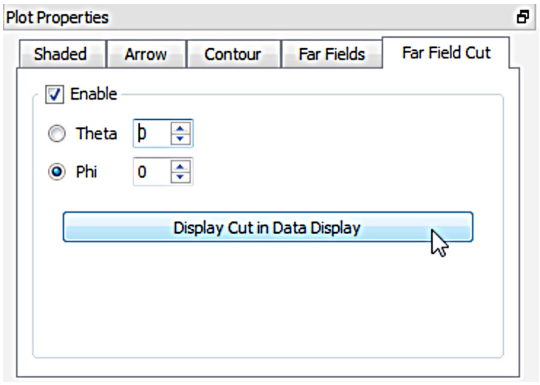


Figure 78.

4. Once done, we will be able to see far field cut in the regular data display as shown below

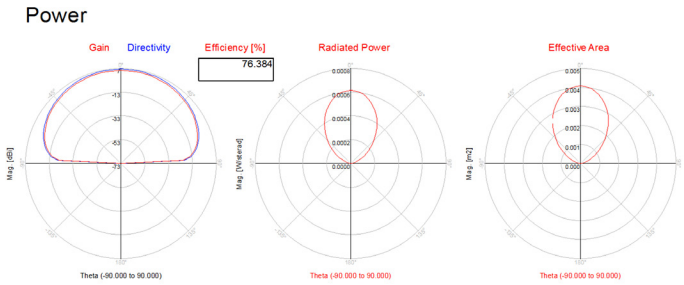


Figure 79.

Case Study 3: EM / Circuit Co-simulation

What is EM / Circuit co-simulation?

Often there is a requirement of having discrete components such as R, L, C, Transistor, Diodes etc. in the layout but EM solvers cannot simulate these discrete components directly, hence we use co-simulation whereby we create a layout component and then place it into the schematic for assembly of discrete components.

Typical process for EM / Circuit co-simulation

1. Connect Pins in the layout where we need to make connections for discrete components
2. Define the stackup and other regular EM settings like Mesh, Simulation Frequency range etc.
3. Create an EM Model and Symbol for this layout component
4. Place this layout component in Schematic and connect the required discrete components
5. Set up the appropriate simulation in schematic. Momentum/FEM simulation will be performed if it is already not done. Otherwise the same data will be reused.

Step 1 - Create a layout where co-simulation needs to be performed

1. Create the layout manually or generate it from the schematic as described in earlier sections.
2. Place Pins wherever we need to make connections or assemble discrete parts along with layout.
3. In this case we have used the “cond” layer for conductors and a “hole” layer for VIA to provide a path to ground.

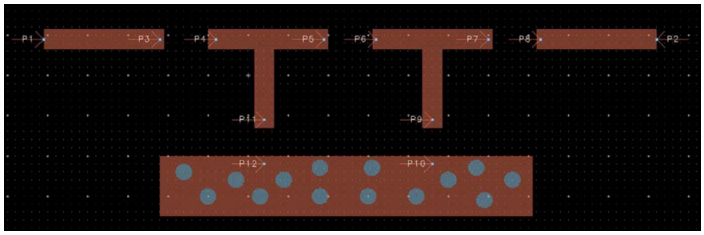


Figure 80.

4. Create a substrate with 25 mil Alumina substrate having *Er=9.9, TanD=0.0009 and* cond layer as Gold with conductivity of *4.1E7* and thickness of *0.7 mil*. The “hole” layer mapped as VIA will also have Gold conductivity as shown in the graphics.

Tip:
To include a VIA in the substrate right-click “Alumina” in the graphics shown on the substrate window and click **Map Conductor VIA**.

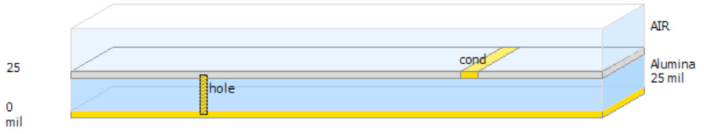


Figure 81.

5. Setup the frequency plan as needed for schematic simulation, e.g. in these case we will keep it from 0.01GHz to 1 GHz with 101 points.

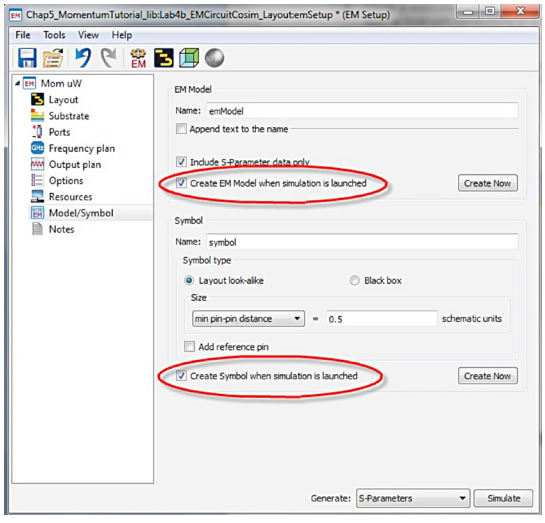


Figure 82.

Note:
If we need to assemble non-linear components such as a Transistor, which needs to be DC–biased, then the Momentum simulation should start from 0 Hz so that DC component can be taken into account accurately.

Step 2 - Create EM / Circuit co-simulation component and symbol

1. For EM / Circuit co-simulation setup, go to the Model/Symbol option and select the **“Create EM Model when...”** and **“Create Symbol when.....”** as shown in the snapshot
2. These options will create an EM database and symbol that can then be used during the EM/Circuit co-simulation
3. Symbol size can be adjusted by setting the **Size->min pin-pin distance** options and by setting the Schematic unit to be 0.1, 0.2 etc...., for this case, we set it to 0.5 to keep the symbol reasonably sized when it is placed in the schematic
4. If you want to perform an EM simulation along with a circuit simulation then click the **Create Now** button for emModel and symbol **or** click the Simulate icon first to perform a Momentum simulation...either way should be fine...
5. Click **Simulate** button to begin Momentum simulation

Step 3 - Simulation and database generation process

1. When we perform a Momentum simulation, a warning as below can be noticed in the status window:

```
The port setup needed to be corrected:
Calibration will not be used for port "P11" (pin
"P11" is not on the edge between a conductive
and a nonconductive region).
```

2. This message is simply stating that calibration cannot be done for ports that are placed inside the structure and normally we can ignore them.

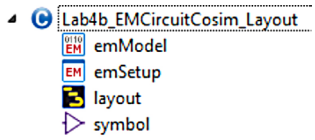


Figure 83.

3. If a specific type of calibration is needed, this can be done in the Ports option of the EM setup window as shown in the snapshot below.

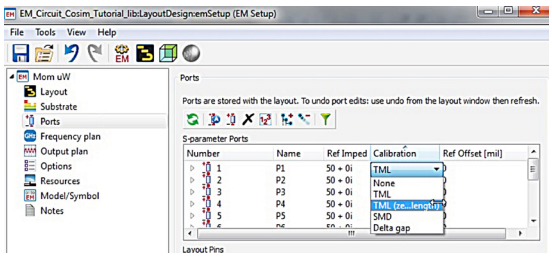


Figure 84.

4. When the simulation is finished, the Momentum data display will be opened but we do not need to see it right now as the discrete components are not yet assembled with the layout. However, sometimes it is good to observe the results to see what kind of cross-coupling exists between the different sections of the layout without the components being mounted. Sometimes we end up having unnecessary coupling between the sections causing our performance to degrade.
5. Observe the ADS main window and we will notice **"emModel"** and **"symbol"** now appearing under the cell on which the simulation is being performed...we will use **"emModel"** for EM / Circuit co-simulation.
6. Open a new schematic cell, drag & drop the **emModel** view from the Main Window on this schematic cell. Select the layout symbol and click **"Choose view for simulation"** and select **emModel** from the list as shown below.

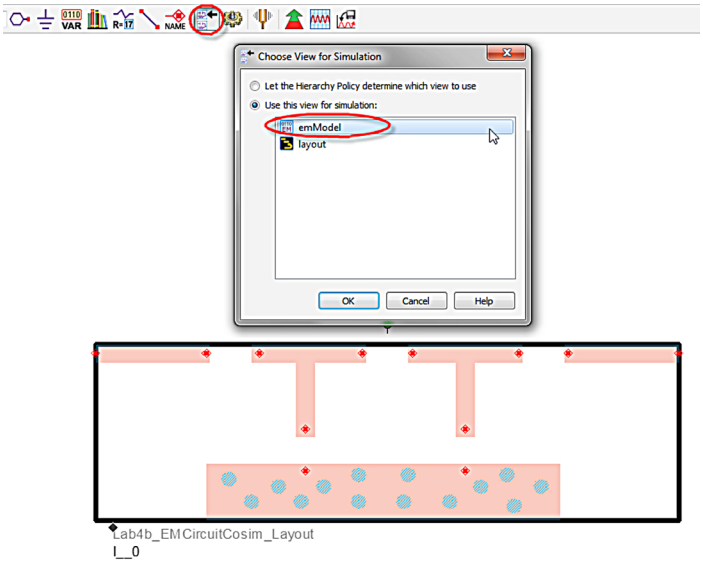


Figure 85.

7. Place the desired discrete components on the schematic and connect them to the layout component as shown in the snapshot below.

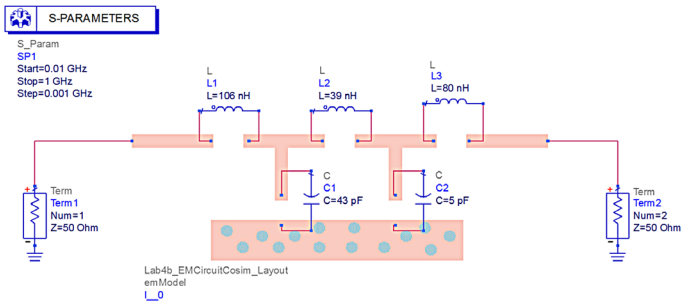


Figure 86.

8. Click the **Simulate** icon on the schematic and insert the rectangular plot to observe S(1,1) & S(2,1) as illustrated.

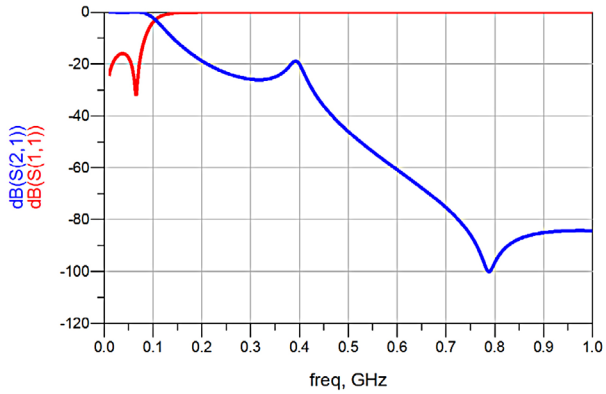


Figure 87.

Using the FEM Simulator in ADS

ADS Licenses Used: Layout, FEM Simulator

Introduction

The FEM simulator provides a complete solution for electromagnetic simulation of arbitrarily-shaped and passive three-dimensional structures. FEM simulators create a full 3D EM simulation and are an attractive option for designers working with RF circuits, MMICs, PC boards, modules, and Signal Integrity applications. It provides fully automated meshing and convergence capabilities for modeling arbitrary 3D shapes such as bond wires and finite dielectric substrates. Along with Momentum, the FEM simulator in ADS provides RF and microwave engineers access to some of the most comprehensive EM simulation tools in the industry.

Developed with the designer of high-frequency/high-speed circuits in mind, the FEM Simulator offers a powerful finite-element EM simulator that solves a wide array of applications with impressive accuracy and speed.

The Finite Element Method

To generate an electromagnetic field solution from which S-parameters can be computed, the FEM Simulator employs the finite element method. In general, the finite element method divides the full problem space into thousands of smaller regions and represents the field in each sub-region (element) with a local function.

In the FEM Simulator, the geometric model is automatically divided into a large number of tetrahedra, where a single tetrahedron is formed by four equilateral triangles.

Representation of a Field Quantity

The value of a vector field quantity (such as the H-field or the E-field) at points inside each tetrahedron is interpolated from the vertices of the tetrahedron. At each vertex, the FEM Simulator stores the components of the field that are tangential to the three edges of the tetrahedron. In addition, the component of the vector field at the midpoint of selected edges that is tangential to a face and normal to the edge can also be stored. The field inside each tetrahedron is interpolated from these nodal values.

Basis Functions

A first-order tangential element basis function interpolates field values from both nodal values at vertices and on edges. First-order tangential elements have 20 unknowns per tetrahedra.

Size of Mesh vs. Accuracy

There is a trade-off between the size of the mesh, the desired level of accuracy, and the amount of available computing resources.

On one hand, the accuracy of the solution depends on the number of the individual elements (tetrahedra) present. Solutions based on meshes that use a large number of elements are more accurate than solutions based on coarse meshes using relatively few elements. To generate a precise description of a field quantity, each tetrahedron must occupy a region that is small enough for the field to be adequately interpolated from the nodal values.

However, generating a field solution for meshes with a large number of elements requires a significant amount of computing power and memory. Therefore, it is desirable to use a mesh that is fine enough to obtain an accurate field solution but not so fine that it overwhelms the available computer memory and processing power.

To produce the optimal mesh, the FEM Simulator uses an iterative process in which the mesh is automatically refined in critical regions. First, it generates a solution based on a coarse initial mesh. Then, it refines the mesh based on suitable error criteria and generates a new solution. When selected, S-parameters converge to within a desired limit and the iteration process ends.

Field Solutions

During the iterative solution process, S-parameters typically stabilize before the full field solution. Therefore, when analyzing the field solution associated with a structure, it may be desirable to use a convergence criterion that is tighter than usual.

In addition, for any given number of adaptive iterations, the magnetic field (H-field) is less accurate than the solution for the electric field (E-field) because the H-field is computed from the E-field using the following relationship:

$$H = \frac{\Delta \times E}{-j\omega\mu}$$

Thus, making the polynomial interpolation function an order lower than those used for the electric field.

Implementation Overview

To calculate the S-matrix associated with a structure, the following steps are performed:

1. The structure is divided into a finite element mesh.
2. The waves on each port of the structure that are supported by a transmission line having the same cross section as the port are computed.
3. The full electromagnetic field pattern inside the structure is computed, assuming that each of the ports is excited by one of the waves.
4. The generalized S-matrix is computed from the amount of reflection and transmission that occurs.

The final result is an S-matrix that allows the magnitude of transmitted and reflected signals to be computed directly from a given set of input signals, reducing the full three-dimensional electromagnetic behavior of a structure to a set of high frequency circuit values.

Setting up an FEM Simulation

Key steps to be followed for a successful FEM simulation in ADS are:

1. Creating a Physical design
2. Defining Substrates
3. FEM Simulation Setup:
    a. Assigning Port Properties
    b. Defining Frequency and output plan
    c. Defining Simulation Options e.g. Meshing, Solver Selection (Direct or Iterative) etc.
    d. Run FEM Simulation
4. View the Results, Far Fields etc.

Case Study: Microstrip Low Pass Filter

Let's learn FEM simulation in ADS by creating simple low pass filter circuit as shown below using MLIN components from TLines-Microstrip library in ADS layout.

Step 1 - Creating a Physical Design

1. Create a new workspace Lab20_FEM_Simulations_wrk and select units as "mm" in the workspace wizard.
2. From the TLines-Microstrip library, place 5 MLIN components with following dimensions:
    a. Line 1, 3, 5: Width = 0.2 mm, Length = 2.5 mm
    b. Line 2, 4: Width = 4.5 mm, Length = 2.5 mm

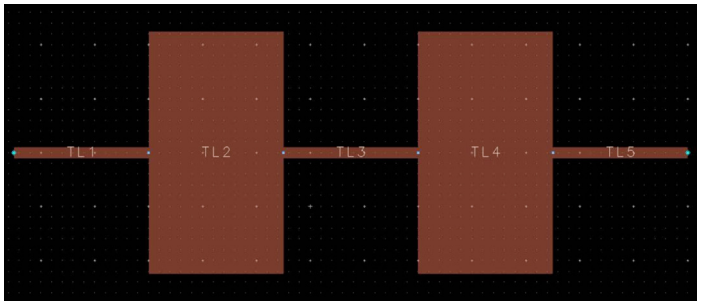


Figure 88.

Step 2 - Defining the Substrate

1. Click the **Substrate** icon as shown here to define the desired substrate for our simulation
2. Select the 25mil Alumina substrate template from the pop-up window and a default substrate will be visible as shown below:

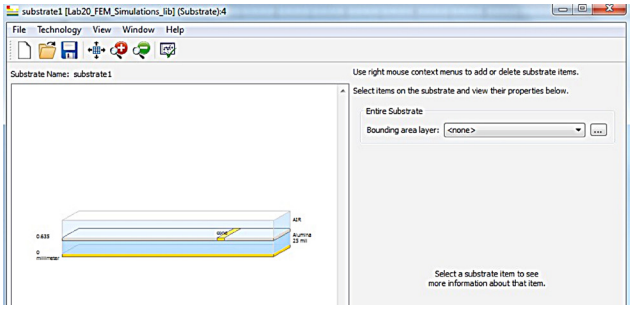


Figure 89.

3. Go to the **Technology > Material Definition** menu and in the **Dielectric** Tab modify the existing Alumina's TanD (Loss Tangent) as *0.0007*. You can also add a dielectric using the **"Add from Database"** option.

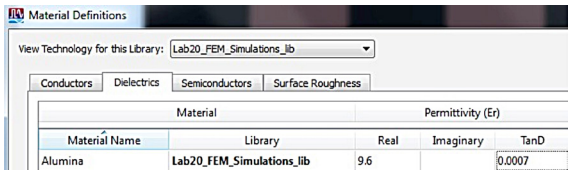


Figure 90.

4. Go to the **Conductors** Tab and click **"Add from Database"** then select **Gold** conductor from the available list and click **OK**.

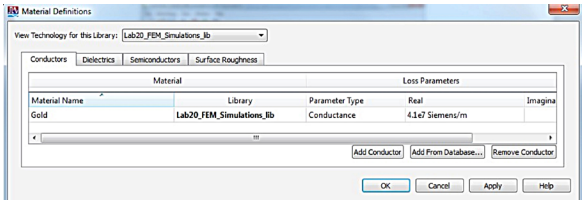


Figure 91.

5. In the GUI of the susbtrate setup, click **cond strip** and modify the Material as "Gold" and enter thickness as *8 micron*.

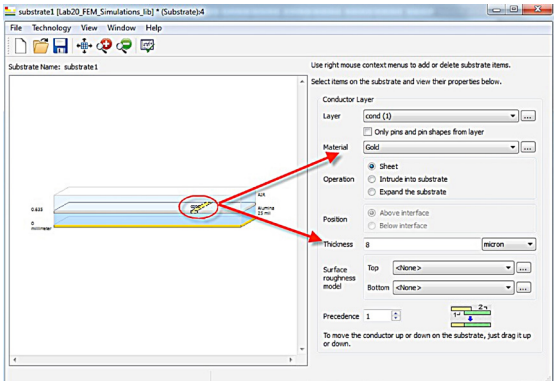


Figure 92.

6. Click **Save** and close the substrate editor.
7. Connect 2 Pins, one each at the input and output connection point using the Pin icon

Step 3 - FEM simulation setup

1. Click the EM Setup icon to open the EM Simulation Setup window. Select FEM Simulator.
2. Select the Frequency Plan option, and enter Fstart = 0.1 GHz; Fstop = 8 GHz.

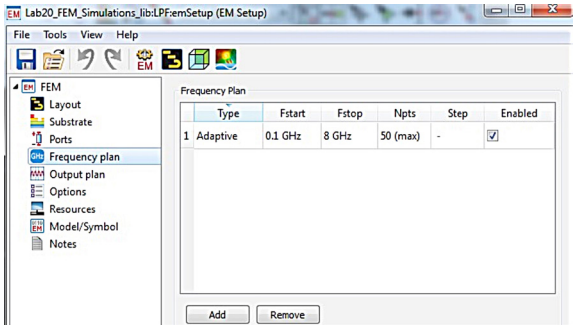


Figure 93.

3. Go to the **Options** Tab which is one of the critical steps in setting up an FEM simulation. Let's discuss each option in detail.
   a. **Physical Model**: As ADS possess a 2D layout editor, we need to define 3D attributes of the structure, which will be used for the FEM simulation in this tab:
      i. Substrate LATERAL extension: This option lets the user decide how much extra dielectric to use for finite dielectric size in from the edge on layout in all directions where Calibrated Ports (TML or TML Zero Length) are not connected.
      ii. Substrate VERTICAL extension: This option lets the user decide the Air height on top of dielectric surface. As a general guideline the vertical extension should be @ 5-10 times of substrate height.

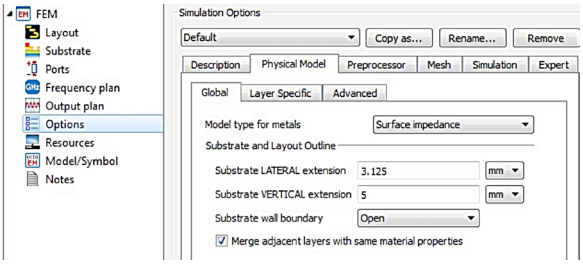


Figure 94.

For our project, we will keep the default settings as shown above.

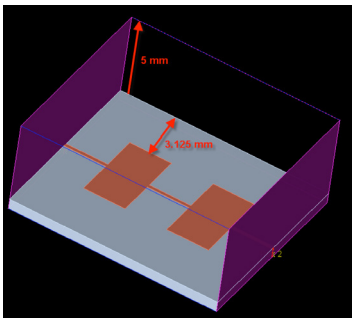


Figure 95.

Lateral extension = 3.125 mm
Vertical extension = 5 mm

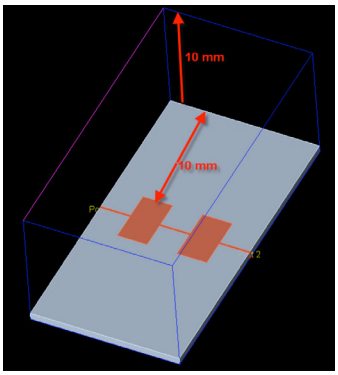


Figure 96.

Lateral extension = 10 mm
Vertical extension = 10 mm

The snapshots above shows 3D views of the filter structure with two LATERAL extension setting.

b. **Mesh**: For FEM simulation, Mesh has various settings that need to be understood properly for accurate simulations.

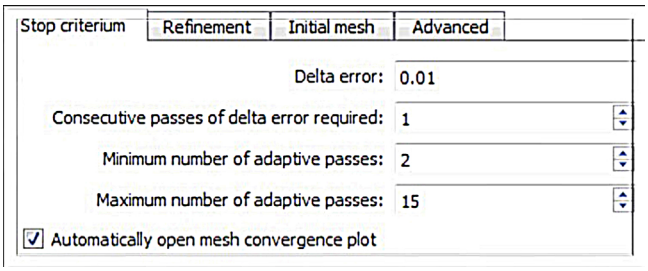


Figure 97.

Stop Criterium:

- **Delta Error**: This figure determines the Mesh convergence factor to have stabilized fields as described in the section "Size of Mesh vs. Accuracy." This is a figure of merit to check S–matrix divergence from one mesh size to another. Once the difference is below the delta error number then the Matrix solution process is started.
- **Consecutive passes of delta error required**: This option lets the user check whether the first mesh convergence achieved was real or not.
- **Minimum number of adaptive passes**: Number of mesh iterations to be performed even if the mesh convergence is achieved earlier than the number specified.
- **Maximum number of adaptive passes**: Maximum limit for mesh iterations to meet the delta error criteria.

Set the parameters as shown in the snapshot above.

Refinement:
Under the refinement tab, designers can specify the frequency at which the Mesh will be generated to solve the structure. As a general guideline for better & quicker mesh convergence it is recommended to create the mesh at the frequency where the structure has a good amount of energy. For filter structures it is recommended that the mesh frequency is in the passband. For our LPF, select Manual selection and enter it as 1 GHz.

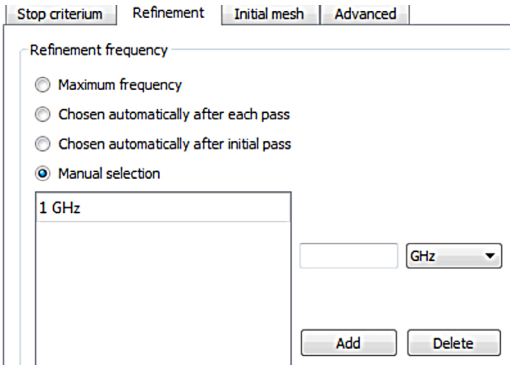


Figure 98.

Initial Mesh:
In the Initial mesh settings the designer can specify a good starting size for the mesh, which can help in getting to convergence faster.

The Automatic Conductor Mesh setting enables the mesher to create a finer mesh along the edges of the strips for better accuracy. This feature is helpful in simulating some troublesome, tightly coupled structures.

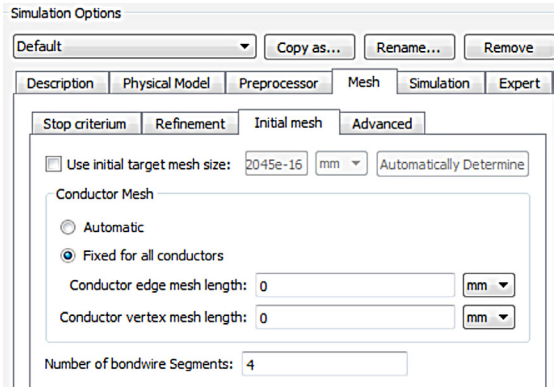


Figure 99.

Advanced:
Under the Advanced option tab, we can specify following:

- **Target Mesh Growth**: Percentage of Tetrahedron growth during each iteration.
- **Use Initial minimal mesh size**: This is again to set user defined size for the mesh for faster convergence.
- **Merge objects with same material**: This option helps in reducing the number of unknowns in a structure for faster simulation.
- **Automatic conductor mesh settings**: If Automatic setting was selected under Initial mesh then these factors will be used for finer meshing.

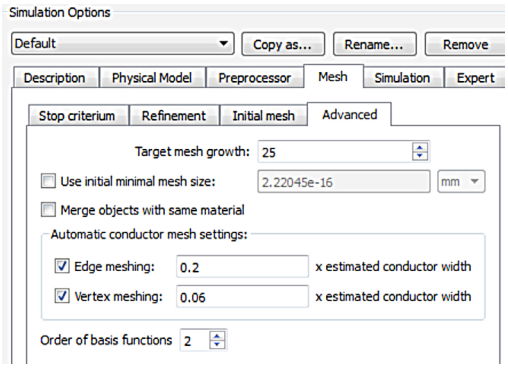


Figure 100.

Click the **Simulate** icon to start the FEM simulation and observe the results as shown below.

Step 4 - Results

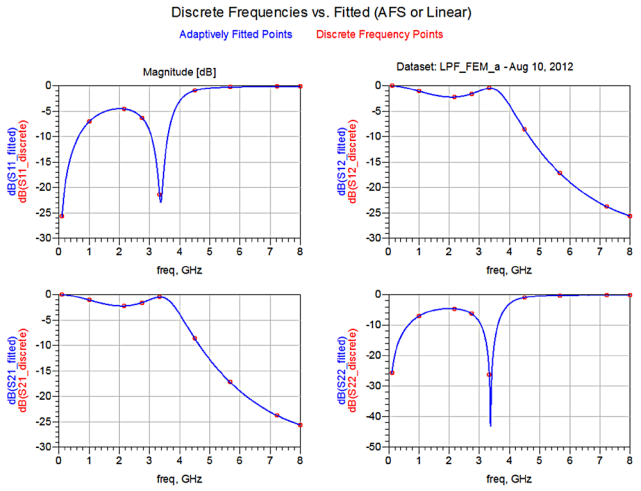


Figure 101.

Click **field visualization**  to open the Field Visualization. Click **View > Top View** to see the top-view of the filter structure.

From the **Plot Properties** tab, select *Z: 0.635* Show button to see the Mesh as illustrated.

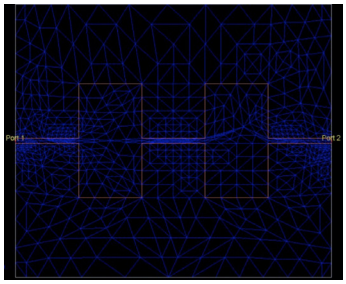


Figure 102.

Mesh with "Fixed for all conductors"

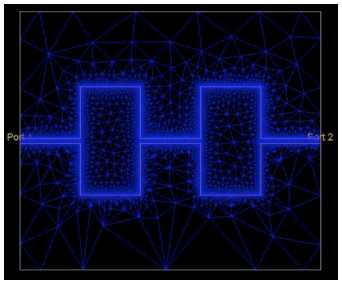


Figure 103.

Mesh with "Automatic" conductor setting

Symmetry Planes in FEM

To reduce the size of the problem and memory requirement for faster simulations, the FEM simulator in ADS can utilize the symmetric boundary condition either in the E-plane or H-plane so that only half of the structure is simulated, thus requiring fewer system resources.

Adding a Symmetry Plane

A symmetry plane defines the boundary on one side of the circuit substrate. Only one box, waveguide, or symmetry plane can be applied to a circuit at a time. When a symmetry plane is defined, the simulation results will be equivalent to the results of a larger circuit that would be created by mirroring the circuit about the symmetry plane.

For symmetric circuits, this enables faster simulations that require less memory because only half the actual structure needs to be simulated.

To add a symmetry plane:

1. Choose **EM > FEM Symmetry Plane > Add Symmetry Plane**.
2. Select the direction of the symmetry plane. To insert the symmetry plane parallel to the x-axis, click X-axis. To insert the symmetry plane parallel to the y-axis, click Y-axis.
3. Insert the symmetry plane using one of the following two methods:
   a. Position the mouse and click to define the location of the symmetry plane.
   b. From the Layout menu bar, select **Insert > Coordinate Entry** and use the Coordinate Entry X and Coordinate Entry Y fields to specify a point on the edge of the substrate.
4. Click **Apply**.

This boundary specifies the edge of the substrate where the plane of symmetry will be applied.

Editing a Symmetry Plane

Once the symmetry plane is applied, you cannot change its location. If you want to change the location or orientation, you must delete the current symmetry plane and add a new one.

Deleting a Symmetry Plane

To delete a symmetry plane:

Select **EM > FEM Symmetry Plane> Delete Symmetry Plane**. The symmetry plane is removed from the layout.

Case Study: LPF Design with Symmetry Plane

Let's simulate our LPF design using a symmetry plane. Follow the process below:

Step 1 - Create partial design

When using a Symmetry Plane, we only need to create half of the geometry, which should be symmetric around the desired X– or Y–axis.

If we observe our LPF design closely we find that it is symmetric around the X-axis as shown below.

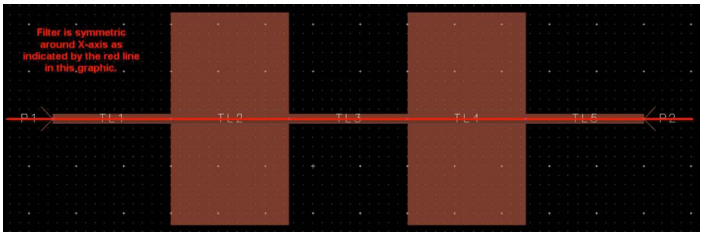


Figure 104.

Using either MLIN or the Rectangle drawing tool, create half of the LPF design as shown below.

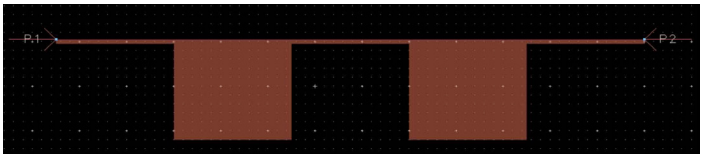


Figure 105.

Input and Output ports will now be connected to the edge where the structure is symmetric as illustrated.

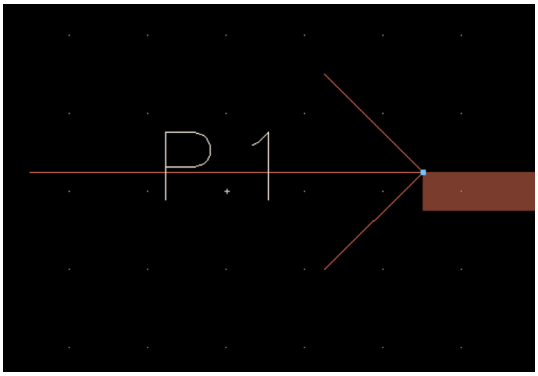


Figure 106.

Step 2 - Applying Symmetry Plane

Go to the **EM > FEM Symmetry Plane > Add Symmetry Plane** option

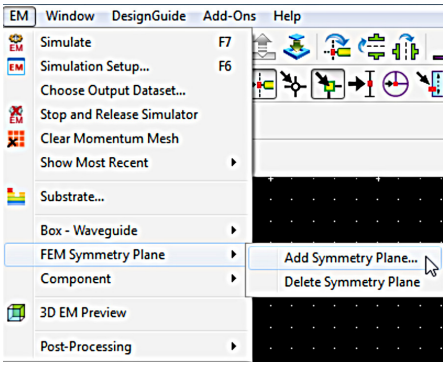


Figure 107.

Select whether you would like to apply the Symmetry Plane on the X-axis or Y-axis from the Add Symmetry Plane dialog box.

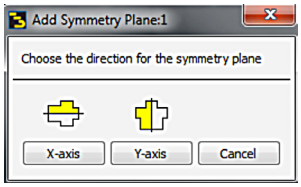


Figure 108.

In our case we will select X-axis. Click the **X-axis** button.

Notice the selection Cross-hair is now available with the mouse cursor. Click either Port 1 or Port 2 to apply the symmetry plane. Once finished it will appear as below.

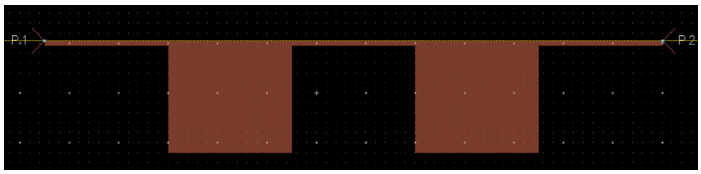


Figure 109.

Note:
The dotted line indicates a symmetry plane is in use.

Step 3 - FEM Simulation

The FEM simulation steps are exactly the same as described earlier. Follow the same steps and run the FEM simulation.

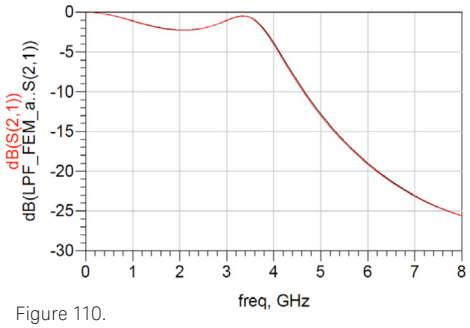


Figure 110.

From above display it can be seen that results for a full structure FEM simulation and one using a Symmetry plane are identical.

Comparing simulation statistics of Full FEM and Symmetry Plane condition:

Full FEM simulation		FEM simulation with symmetry plane
INITIAL MESH		INITIAL MESH
nbPoints	188	144
nbTetrahedra	618	419
@Delta Error	< 0.01	< 0.01
nbTetrahedra	4378	2145
Solver Time	2 m 39 s	1 m 47 s

Note:

1. In this case we do not see great improvement in terms of solver time because of the simple nature of the structure, but with more complex problems this difference would be appreciable.
2. Simulations are run on 2GHz, Intel Dual core PC with 4GB RAM.
3. Statistics indicated here might change with the software release because of the modification of the internal simulator and mesh algorithms etc.

For more details on the FEM simulator in ADS, refer to the Electromagnetic chapter of the ADS documentation.

RF System Design

ADS Licenses Used: RF System Simulation

Keysight ADS provides all the necessary capabilities to perform RF system design and simulations. RF system design is an important and critical step to validate the system performance for first pass success. RF system architecture can be implemented using RF System models available in the Analog/RF library as shown here.

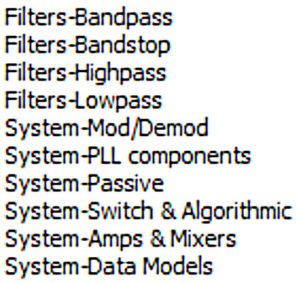


Figure 111.

The library names are self-explanatory and designers can select the desired component from the respective library for their system design. It is also recommended to read the system components documentation for a better understanding of the component's behavior, its limitations and recommended simulator to be used for simulation.

Case Study 1: Receiver System Design

1. Create a new workspace Lab5_RF_System_Design_wrk and open a new schematic cell and name it as Lab5a_RFSystemDesign.
2. Place Amp and Mixer2 from the System-Amps & Mixers library and set their characteristics as shown below.

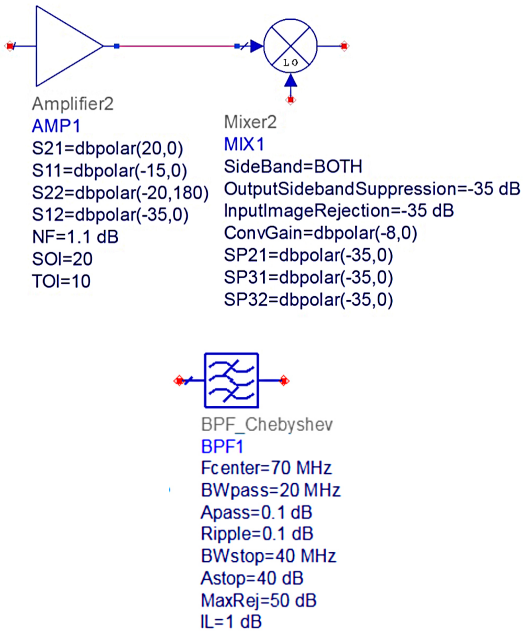


Figure 112.

3. Place the Chebyshev Bandpass filter component at the Mixer output from Filters-Bandpass library and set its characteristics as illustrated.
4. Copy and paste the Amplifier twice after the BPF component and change the following specifications (these will be used as 2-stage IF Amplifiers)
   a. TOI=20
   b. SOI=30
   c. NF=3 dB

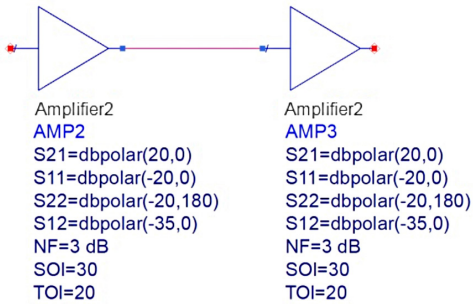


Figure 113.

5. Once completed, the schematic will look similar to the one shown below.

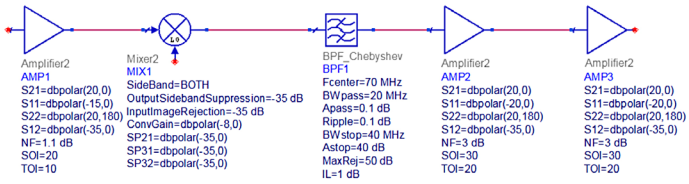


Figure 114.

6. Now, our job remaining is to connect the RF and LO sources and setup the simulation to observe the system response. Place **P_1Tone** and Osc source from the **Sources-Freq Domain** library and set their characteristics as illustrated (Notice the PhaseNoise list in the Osc source.).

Connect P_1Tone at the Receiver input and Osc at the LO terminal of the Mixer component.

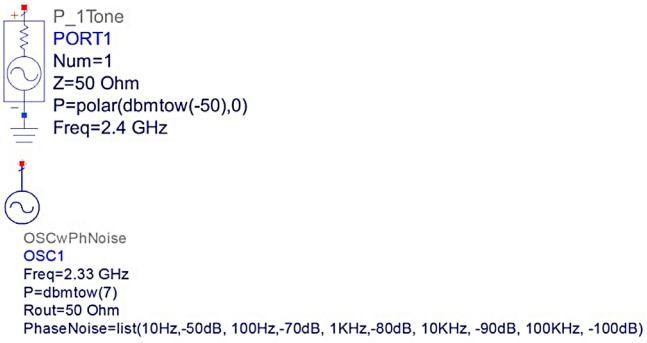


Figure 115.

7. Place the **HB simulation controller** from the **Simulation-HB** library and set its characteristics as show below.

Tip:
Please follow general convention for simulations involving more than 1 source (or tones); the frequency with more power should be defined first i.e. frequency components should appear in descending order on a power basis. If tones or sources have equal power then designers can decide which frequency to define first.

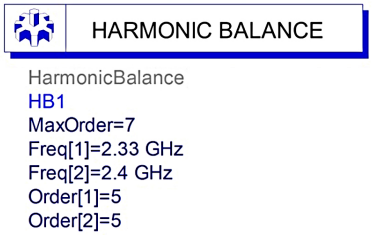


Figure 116.

8. Place a **Term** component at the output (after the 2nd IF amplifier) and click **Wire Label** and enter *"vout"* in the pop-up window and click the "+" terminal of the Term component.

9. Once completed the receiver system diagram would look as below.

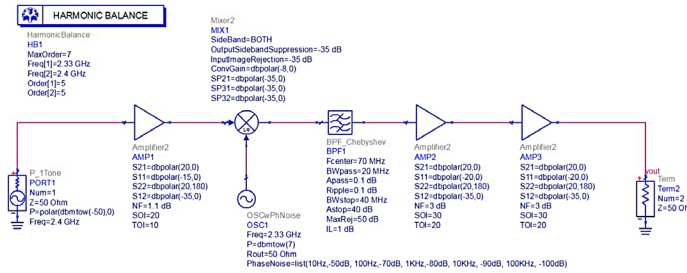


Figure 117.

10. Save the design and click the **Simulate** icon. Insert a srectangular graph in the data display window, add *"vout"* from the measurement list and select *"Spectrum in dBm"* to observe the output spectrum.

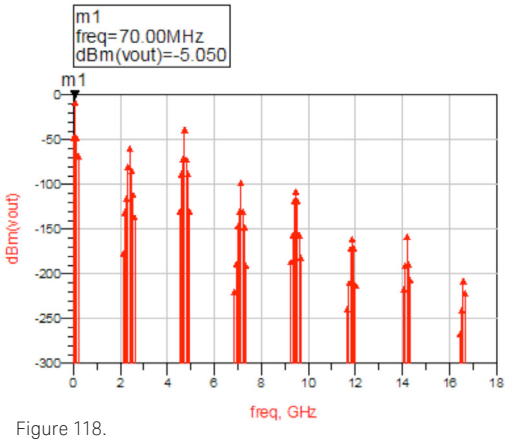


Figure 118.

Additional Note:
Try placing a Wire Label at various points and observe the spectrum at those nodes.

Case Study 2: Phase Noise Simulation

Phase noise is an important simulation for receiver systems and the example below shows how to perform Phase noise analysis using Harmonic Balance simulator in ADS.

1. Right-click **Lab5a_RFSystemDesign** and click **Copy Cell**.
2. In the pop-up window, give new name as Lab5b_RFSystemDesign_PhaseNoise.
3. Open the schematic design for this newly copied cell and from Simulation-HB library place NoiseCon (Noise Controller) block onto schematic.

4. Double-click to open the properties of NoiseCon and set the following parameters:
   a. Freq tab:
      i. Sweep Type = Log
      ii. Start = 10 Hz, Stop = 100 KHz
      iii. Num. of pts. will automatically become 5, indicating 5 noise analysis frequencies, i.e. 10 Hz, 100Hz, 1KHz, 10KHz and 100KHz, which is the same as we are specifying in the Oscillator used as an LO source in the system
   b. Nodes tab:
      i. Select Pos Node = *vout* from the drop down box, which is the output node where we provided a label in the earlier lab exercise.
      ii. Click **Add**
   c. Phase Noise Tab:
      i. Phase Noise Type = Phase Noise Spectrum
      ii. Under Specify Phase Noise Carrier specify Frequency as *70 MHz*, alternatively we can also specify Carrier mixing indices such as *{-1,1}* etc.
5. Click **OK** and now our Noise Controller is setup nicely, we have one extra step in linking this Noise Controller to our HB simulation controller.
6. Double-click **HB controller**, and go to the **Noise** Tab.
   a. Check **Noise Cons** option
   b. From Edit drop-down box select NC1 (name of Noise controller)
   c. Click **Add**
   d. Click **OK** and close the HB simulation controller properties box.
7. Run **simulation** and a new data display window will come up. Insert a new rectangular plot and select "vout" to be plotted in dBm to see the same spectrum as in the earlier lab.

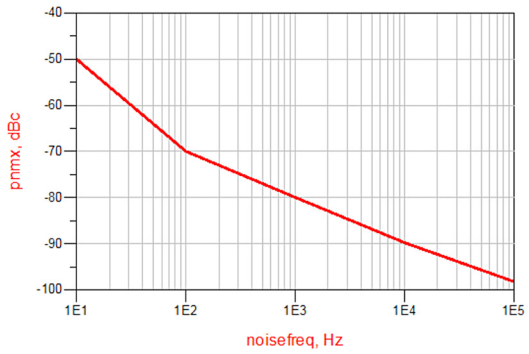


Figure 119.

8. Insert a new rectangular plot, select "pnmx" (i.e. Phase Noise) to be plotted and from Plot Options change the X-axis to Log. Click OK to see the Phase Noise plot at various offsets.

Case Study 3: 2-Tone Simulation of the Receiver System

Performing a 2-tone simulation is also of specific importance for system level analysis and the example here shows how to perform 2-tone simulations on frequency converting based systems.

1. Right-click **Lab5a_RFSystemDesign** and click **Copy Cell**
2. In the Pop-up window, enter the name as Lab5c_RFSystemDesign_2Tone and click OK
3. Open the schematic of the newly copied cell. For a 2-tone simulation we need to change the P_1Tone source, which is currently used for the RF source. Delete the 1-tone source and from the **Sources-Freq Domain** library place a **P_nTone** source on the schematic.
4. Double-click the P_nTone source and edit the properties as below:
   a. Click **Freq[1]** and enter the frequency as 2.399 GHz, click **Apply**.
   b. Click **Add** button to add a 2nd tone frequency with the name Freq[2] and enter the frequency as 2.401 GHz, click **Apply**.
   c. Click **P[1]**, which is the power in the 1st tone, enter the power as polar(dbmtow(-50),0) and click **Apply**.
   d. Click **Add** button to add power for the 2nd tone and enter the same power as for the 1st tone. Please note that for a 2-tone test it is mandatory to have the same power in both of the tones otherwise the analysis will not be valid.
5. Now, since we have 3 source frequencies in the schematic, we need to modify the HB simulator to specify these 3 frequencies for proper mixing product calculations. Double-click the HB controller and specify 3 frequencies in order as following:
   a. Freq[1] = 2.33 GHz
   b. Freq[2] = 2.399 GHz
   c. Freq[3] = 2.401 GHz
6. Click the **Simulate** button to run the simulation and then zoom using the graph zoom icon on the data display near 70MHz to see the 2-tone simulation results as shown below.

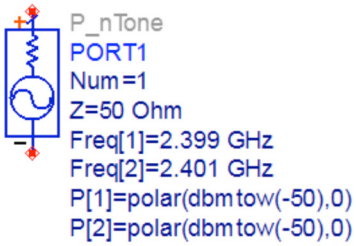


Figure 120.

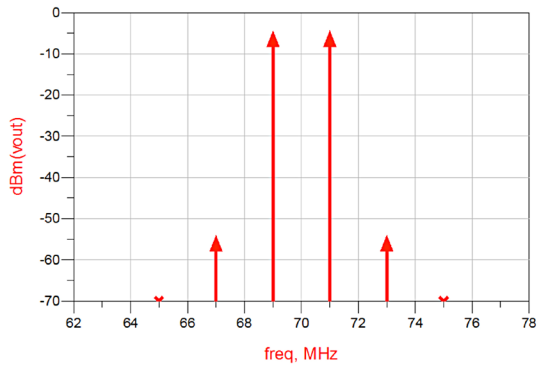


Figure 121.

Case Study 4: RF System Budget Analysis

Performing RF System Budget is very useful to characterize the system behavior and analyze how a system behaves as the signal transitions from each component. The easiest way to perform RF System Budget analysis is by using the Budget Controller, which offers more than 40 built-in budget measurements offering great ease-of-use.

One of the fundamental rules to follow while using the Budget Controller is that the system should only have 2-port components with the exception of S2P files, and an AGC Amplifier with Power Control. The ADS Simulation-Budget library provides a special Mixer with an Internal LO so that super-heterodyne systems can be analyzed.

Step 1 - Modifying the RF system design

1. Copy the **Lab5a_RFSystemDesign** cell by right clicking and selecting Copy Cell and provide the new name as **Lab5d_RFSystemDesign_Budget**.

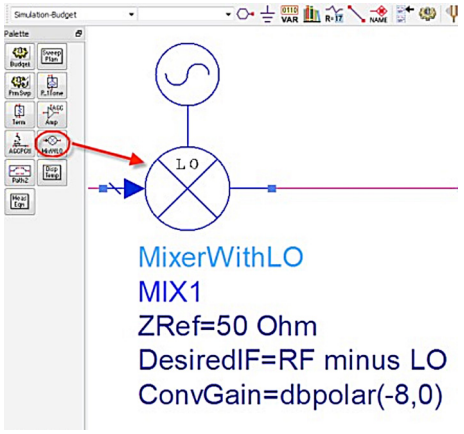


Figure 122.

2. In order to perform budget analysis on our receiver system, we need to replace the Mixer and LO source component with the Mixer with LO component from the Simulation-Budget library as shown here.
   Modify the following parameters-
   ConvGain=dbpolar(-8,0)
   Desired IF = RF minus LO
3. Delete the HB controller and insert the Budget controller from the Simulation-Budget library, double-click it and modify the parameters under the Setup tab as shown below. From the measurements tab select the measurements as shown below (namely: Cmp_NF_dB, Cmp_OutP1 dB_dBm, NF_Refln_dB, OutTOI_dBm, OutSOI_dBm).

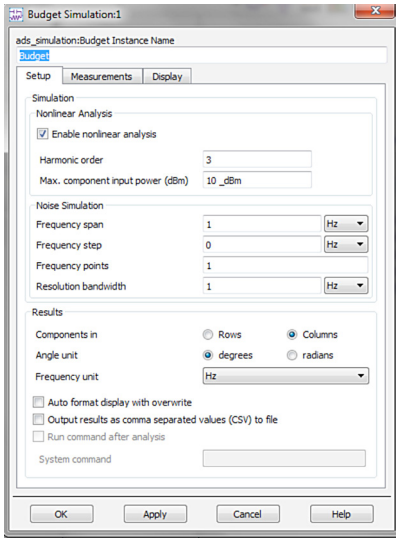


Figure 123.

Step 2 - Perform Budget Analysis

1. The overall schematic should look similar to the one shown below, click **Simulate** button.

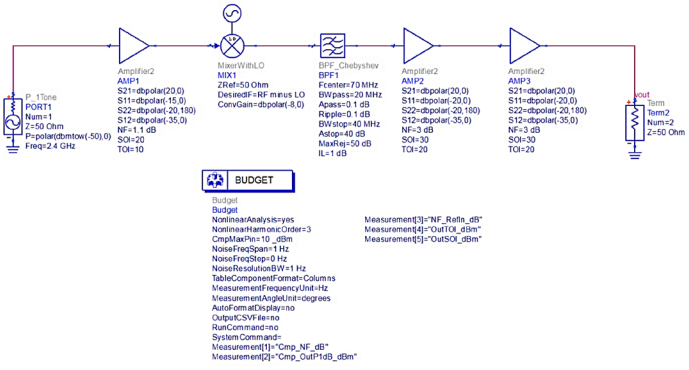


Figure 124.

Insert a Rectangular graph on the data display page. Select **OutTOI_dBm** from the measurement list, click the **Add Vs>>** button and select Cmp_RefDes to plot the budget measurement results vs. component names so that it is easier to see results vs. Component Names as used in the RF System design schematic. (*Notice the X-axis that should display the name of the system components*)

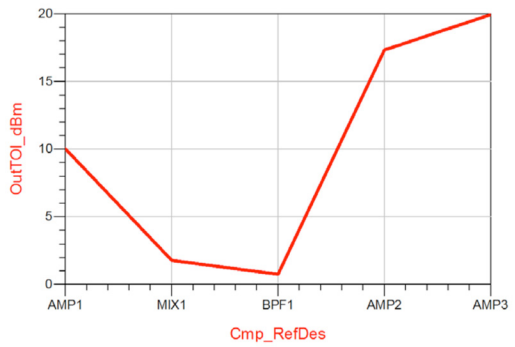
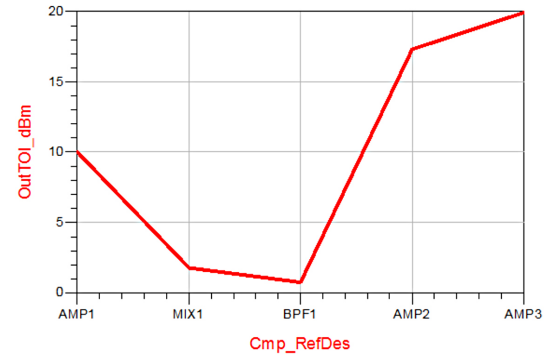


Figure 125.

2. Similarly add OutSOI_dBm, Cmp_OutP1 dB_dBm, NF_Refln_dB vs. Cmp_ResDes to see the different budget measurements as illustrated.



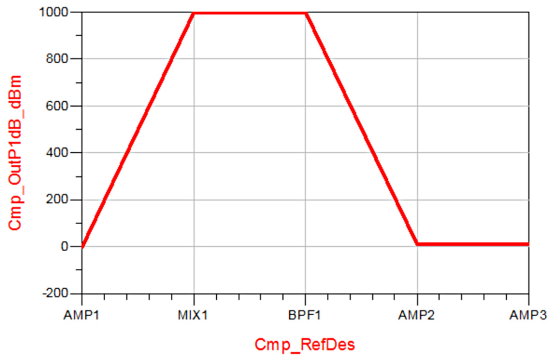


Figure 126.

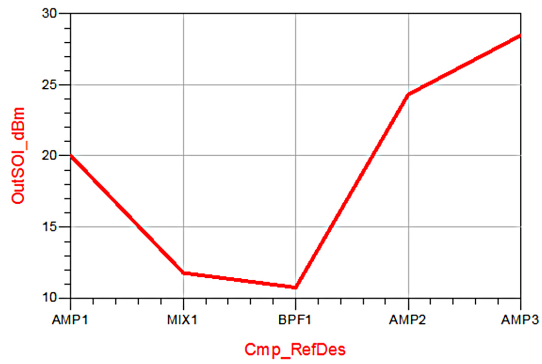


Figure 127.

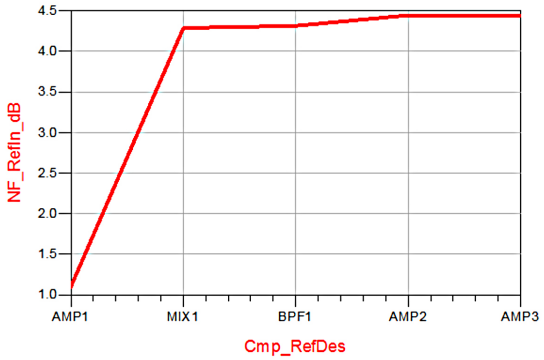


Figure 128.

Question: Why is the Receiver's Noise Figure @4.5dB? Is it too high or as expected?

Try comparing it against theoretical calculations using a Cascaded Noise Figure equation.

Case Study 5: Exporting RF Budget Analysis Results to Excel

The ADS budget controller allows exporting the budget simulation results to Microsoft Excel. In order to activate this feature, double click **Budget Controller** and select the options as shown below. Also, we need to enter the path to Excel.exe as per our installation.

For the case below it is ***C:\Program Files (x86)\Microsoft Office\Office12\Excel.exe***

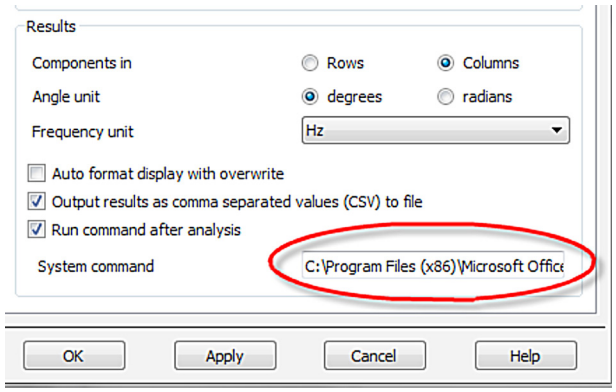


Figure 129.

Click the **Simulate** icon to see Excel open with our budget simulation results. Scroll down the Excel sheet and notice the budget simulation results as shown in the snapshot below.

42	Meas_Name	AMP1	MIX1	BPF1	AMP2	AMP3
43	Cmp_NF_dB	1.131617	8.036397	1.021553	3.021827	3.021827
44	Cmp_OutP1dB_dBm	-0.63804	1000	1000	9.366897	9.366965
45	NF_Refln_dB	1.1	4.285689	4.312709	4.441894	4.443175
46	OutTOI_dBm	10	1.755889	0.729914	17.30733	19.91895
47	OutSOI_dBm	20	11.75589	10.72991	24.30329	28.46084
48						

Figure 130.

Microwave Discrete and Microstrip Filter Design

ADS Licenses Used: Linear Simulation, Momentum Simulation and Layout

Theory

Microwave filters play an important role in any RF front end for the suppression of out of band signals. In the lumped and distributed form, they are extensively used for both commercial and military applications. A filter is a reactive network that passes a desired band of frequencies while almost stopping all other bands of frequencies. The frequency that separates the transmission band from the attenuation band is called the cut-off frequency and denoted as fc. The attenuation of the filter is denoted in decibels or nepers. A filter in general can have any number of pass bands separated by stop bands. They are mainly classified into four common types, namely lowpass, highpass, bandpass and band stop filters.

An ideal filter should have zero insertion loss in the pass band, infinite attenuation in the stop band and a linear phase response in the pass band. An ideal filter cannot be realizable as the response of an ideal low pass or band pass filter is a rectangular pulse in the frequency domain. The art of filter design necessitates compromises with respect to cutoff and roll off. There are basically three methods for filter synthesis. They are the image parameter method, Insertion loss method and numerical synthesis. The image parameter method is an old and crude method whereas the numerical method of synthesis is newer but cumbersome. The insertion loss method of filter design on the other hand is the optimum and more popular method for higher frequency applications. The filter design flow for insertion loss method is shown below.

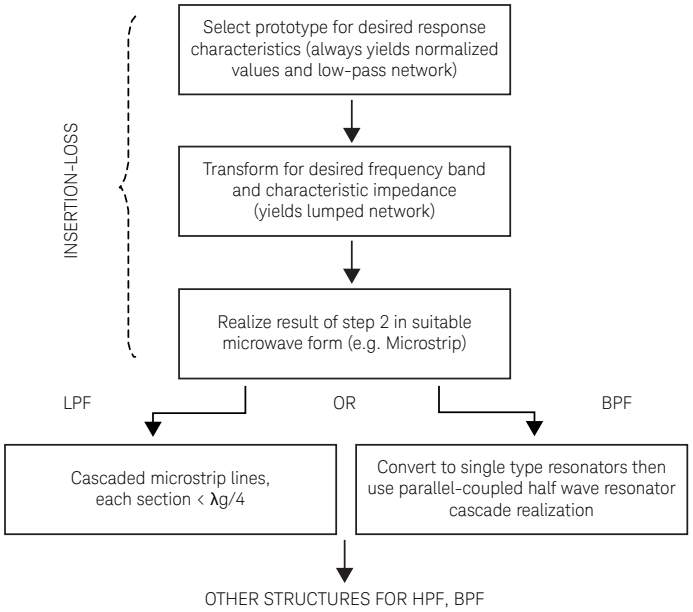


Figure 131.

Since the characteristics of an ideal filter cannot be obtained, the goal of filter design is to approximate the ideal requirements within an acceptable tolerance. There are four types of approximations namely Butterworth or maximally flat, Chebyshev, Bessel and Elliptic approximations. For the proto type filters, maximally flat or Butterworth provides the flattest pass band response for a given filter order. In the Chebyshev method, sharper cutoff is achieved and the pass band response will have ripples of amplitude $1+k^2$. Bessel approximations are based on the Bessel function, which provides sharper cutoff and Elliptic approximations results in pass band and stop band ripples. Depending on the application and the cost, the approximations can be chosen. The optimum filter is the Chebyshev filter with respect to response and the bill of materials. Filter can be designed both in the lumped and distributed form using the above approximations.

Design of Microwave Filters

The first step in the design of Microwave filters is to select a suitable approximation of the prototype model based on the specifications.

Calculate the order of the filter from the necessary roll off as per the given specifications. The order can be calculated as follows:

Butterworth Approximation:

$$L_A(\omega') = 10\log_{10}\{1+\varepsilon(\omega'/\omega_c)^{2N}\}$$

Where $\varepsilon = \{\text{Antilog}_{10} L_A/10\} - 1$ and L_A= 3dB for Butterworth

Chebyshev Approximation:

$$L_A(\omega') = 10\log_{10}\left\{1+\varepsilon\cos^2\left[n\cos^{-1}\left(\frac{\omega'}{\omega_1'}\right)\right]\right\} \quad \text{when} \quad \omega' \leq \text{ and}$$

$$L_A(\omega') = 10\log_{10}\left\{1+\varepsilon\cosh^2\left[n\cosh^{-1}\left(\frac{\omega'}{\omega_1'}\right)\right]\right\} \quad \text{when} \quad \omega' \geq \omega_1'$$

Where, ω_c is the angular cutoff frequency

ω' is the angular attenuation frequency

$L_A(\omega')$ is the attenuation at ω'

N is the order of the filter

$\varepsilon = \{\text{Antilog}_{10} L_{Ar}/10\} - 1$ and L_{Ar} = Ripple in passband

The next step in the filter design is to calculate the prototype values of the filter depending on the type of approximation. The prototype values for the Chebyshev and Butterworth approximations can be calculated using the given equations.

Butterworth Approximation:

$g0 = 1$,

$g_k = 2\sin\{(2k-1)\pi/2n\}$ where $k = 1,2,....n$ and

$g_{N+1} = 1$

Where, n is the order of the filter

Chebyshev Approximation:

The element values may be computed as follows

$$\beta = \ln\left(\coth\frac{L_{Ar}}{17.37}\right)$$ L_{Ar} is the ripple in the passband

$$\gamma = \sinh\left(\frac{\beta}{2n}\right)$$

$$a_k = \sin\left[\frac{(2^k)-1\,\pi}{2n}\right]$$, k=1, 2, 3....n

$$b_k = \gamma^2 + \sin^2\left(\frac{k\pi}{n}\right)$$, k=1, 2, 3....n

$$g_1 = \frac{2a_1}{\gamma}$$

$$g_k = \frac{4a_{k-1}a_k}{b_{k-1}g_{k-1}}$$, k=2, 3.....n

g_{n+1}=1 for n odd

$= \coth^2\left(\frac{\beta}{4}\right)$ for n even.

After computing the prototype values the prototype filter has to be transformed with respect to frequency and impedance to meet the specifications. The transformations can be done using the following equations.

For Lowpass filter:
After Impedance and frequency scaling:

$C'_k = C_k/R_0\,\omega_c$

$L'_k = R_0L_k/\omega_c$ Where $R_0 = 50\Omega$

For the distributed design, the electrical length is given by:

Length of capacitance section: $Z_l/R_0\,C_k$,
Length of inductance section: $L_k\,R_0/Z_h$

Where, Z_l is the low impedance value and Z_h is the high impedance value

For bandpass filter:
Impedance and frequency scaling:

$L'_1 = L_1Z_0/\omega_0\Delta$

$C'_1 = \Delta / L_1Z_0\,\omega_0$

$L'_2 = \Delta\,Z_0/\omega_0C_2$

$C'_2 = C_2/Z_0\,\Delta\,\omega_0$

$L'_3 = L_3Z_0/\omega_0\,\Delta$

$C'_3 = \Delta / L_3Z_0\,\omega_0$

Where, Δ is the fractional bandwidth $\Delta = (\omega_2 - \omega_1)/\omega_0$

Simulation of a Lumped and Distributed Lowpass Filter Using ADS

Typical Design

Cutoff Frequency (f_c)	: 2 GHz
Attenuation at (f = 4 GHz)	: 30dB (LA(ω))
Type of Approximation	: Butterworth

Order of the filter:

$$LA(\omega) = 10\log_{10}\{1+\varepsilon\,(\omega/\omega_c)^{2N}$$

Where,

$$\varepsilon = \{\text{Antilog}_{10}\,LA/10\} - 1$$

Substituting the values of LA (ω), ω and ω_c, the value of N is calculated to be 4.

Prototype Values of the Lowpass Filter:

The prototype values of the filter is calculated using the formula given by

$g_0 = 1$,

$g_k = 2\sin\{(2k-1)\pi/2N\}$ where $k = 1,2,....N$

and $g_{N+1} = 1$

The prototype values for the given specifications of the filter are

g1 = 0.7654 = C_1, g2 = 1.8478 = L_2, g3 = 1.8478 = C_3 & g4 = 0.7654 = L_4

Lumped Model of the Filter

The Lumped values of the Lowpass filter after frequency and impedance scaling are given by

$C_k' = C_k / R_0 \omega_c$

$L_k' = R_0 L_k / \omega_c$ where R_0 is 50Ω

The resulting lumped values are given by C_1 = 1.218 pF, L_2 = 7.35 nH, C_3 = 2.94 pF and L_4 = 3.046 nH

Distributed Model of the Filter

For distributed design, the electrical length is given by

Length of capacitance section (βLc) : $C_k Z_l / R_0$,

Length of inductance section (βLi) : $L_k R_0 / Z_h$

Where,

Z_l is the low impedance value,

Z_h is the high impedance value,

R_0 is the Source and load impedance,

ω_c is the desired cutoff frequency

If we consider Z_l = 10Ω and Z_h = 100Ω then βLc_1 = 0.153, βLi_2 = 0.9239,

βLc_3 = 0.3695 and βLi_4 = 0.3827

Since $\beta = 2\pi/\lambda$, the physical lengths are given by

Lc_1 = 1.68 mm,

Li_2 = 10.145 mm,

Lc_3 = 4.057 mm and

Li_4 = 4.202 mm.

Schematic Simulation Steps for Lumped Low Pass Filter

1. Open the Schematic window of ADS.
2. From the Lumped Components library select the appropriate components necessary for the lumped filer circuit. Click the necessary components and place them on the schematic window of ADS as illustrated.

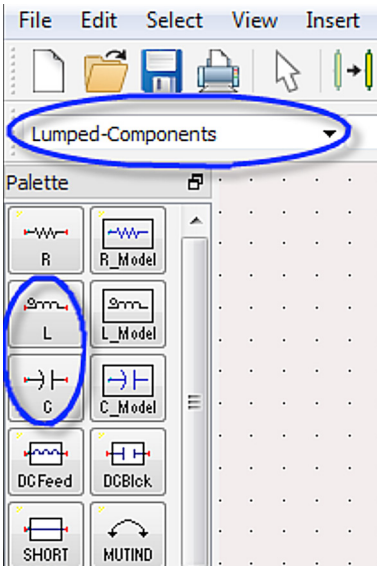


Figure 132.

3. Create the lumped model of the lowpass filter on the schematic window with appropriate lumped components and connect the circuit elements with wire . Enter the component values as calculated earlier.
4. Terminate both ports of the lowpass filter using terminations selected from the Simulation-S_Param library.
5. Place the S-Parameter simulation controller from the Simulation-S_Param library and set its parameters as:
   Start = 0.1 GHz
   Stop = 5 GHz
   Number of Points=101 (or enter Step Size = 49 MHz)

This completes the lumped model design of the filter as shown in the figure below.

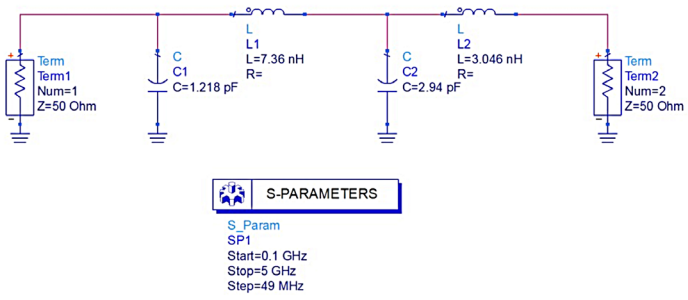


Figure 133.

6. Simulate the circuit by clicking **F7** or the simulation gear icon.
7. After the simulation is complete, ADS automatically opens the Data Display window displaying the results. If the Data Display window does not open, click **Window > New Data Display**. In the data display window, select a rectangular plot and this automatically opens the place attributes dialog box. Select the traces to be plotted (in our case S(1,1) & S(2,1) are plotted in dB) and click **Add**>>.
8. Click and insert a marker on S(2,1) trace around 2GHz to see the data display graph as shown below.

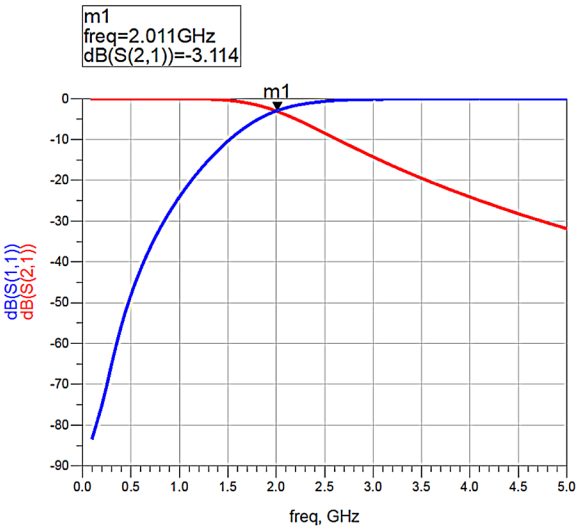


Figure 134.

Results and Observations:

It is observed from the schematic simulation that the lumped model of the lowpass filter has a cutoff of 2 GHz and a roll off as per the specifications.

Layout Simulation Steps for Distributed Low Pass Filter

Calculate the physical parameters of the distributed lowpass filter using the design procedure given above. Calculate the width of the Z_l and Z_h transmission lines for the design of the stepped impedance lowpass filter. In this case Z_l = 10Ω and Z_h = 100Ω and the corresponding line widths are 24.7 mm and 0.66mm respectively for a dielectric constant of 4.6 and a thickness of 1.6 mm.

Calculate the length and width of the 50 Ω line using the line calc (Tools->Line Calc->Start Line Calc) window of ADS as shown in figure below.

50 Ω Line input & output connecting line:

Width: 2.9 mm

Length: 4.5 mm

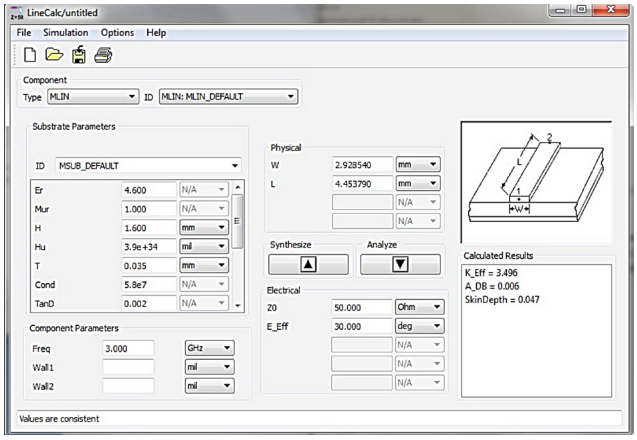


Figure 135.

Create a model of the lowpass filter in the layout window of ADS. The Model can be created by using the available library components **or** by drawing rectangles.

To create the model using library components, select the **TLines–Microstrip** library. Select the appropriate Microstrip line from the library and place it on the layout window as shown.

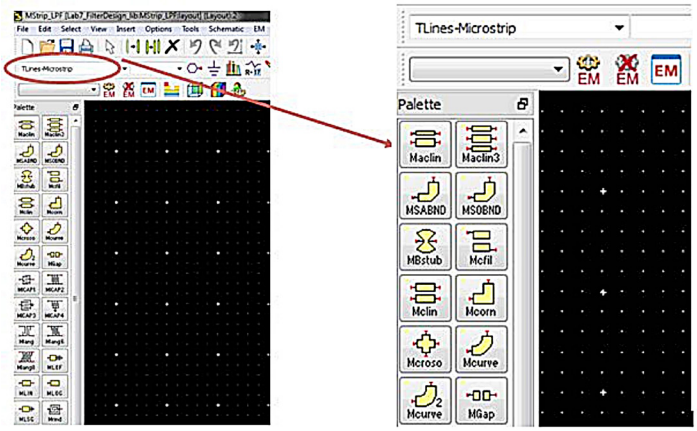


Figure 136.

Complete the model by connecting the transmission lines to form the stepped impedance lowpass filter as shown below based on the width & length calculations done earlier.

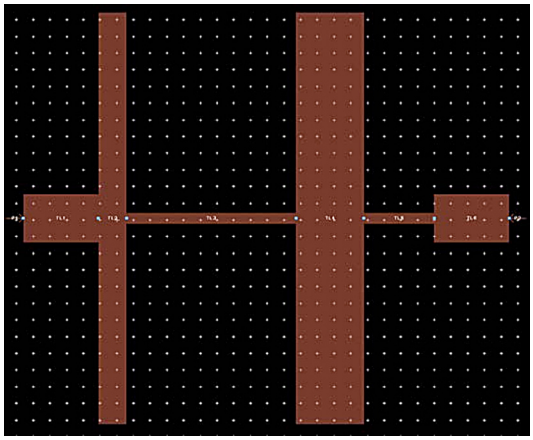


Figure 137.

Connect Pins at the input & output and define the substrate stackup and setup the EM simulation as described in the EM simulation chapter earlier. We shall use the following properties for the stackup:

Er=4.6
Height = 4.6 mm
Loss Tangent = 0.0023
Metal Thickness = 0.035 mm
Metal Conductivity = Cu (5.8E7 S/m)

In the EM setup window, go **to Options > Mesh** and turn on Edge Mesh.

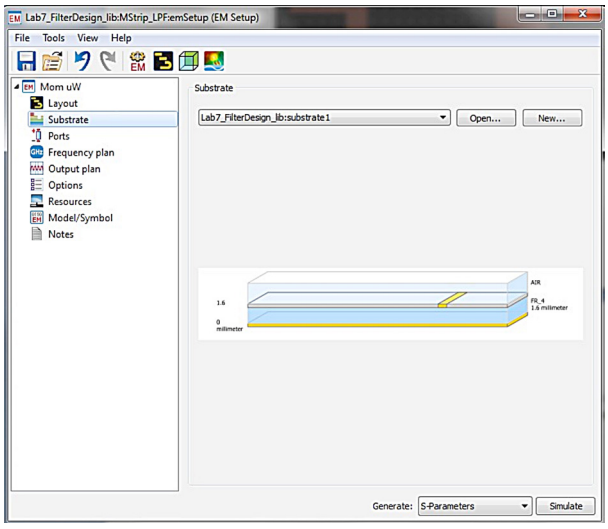


Figure 138.

Click the **Simulate** button and observe the S11 and S21 response

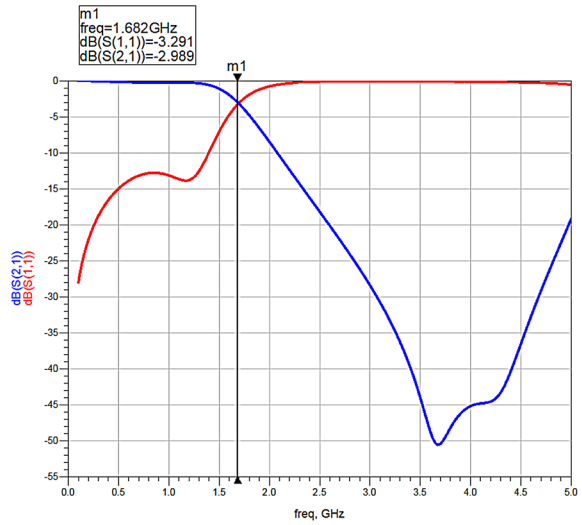


Figure 139.

It can be noted that the 3dB cut-off has shifted to 1.68GHz instead of 2 GHz as our theoretical calculations doesn't allow accurate analysis of open end effect and a sudden impedance change in the transmission lines, hence the lengths of the lines needs to optimized to recover the desired 2GHz cutoff frequency specifications.

This optimization can be carried out using the Momentum simulator in ADS or by performing a parametric sweep on the lengths of Capacitive and Inductive lines.

Parametric EM Simulations in ADS 2011

To begin parametric simulation on the layout, we need to define the variable parameters that shall be associated with the layout components. Click **EM > Component > Parameters** as shown below

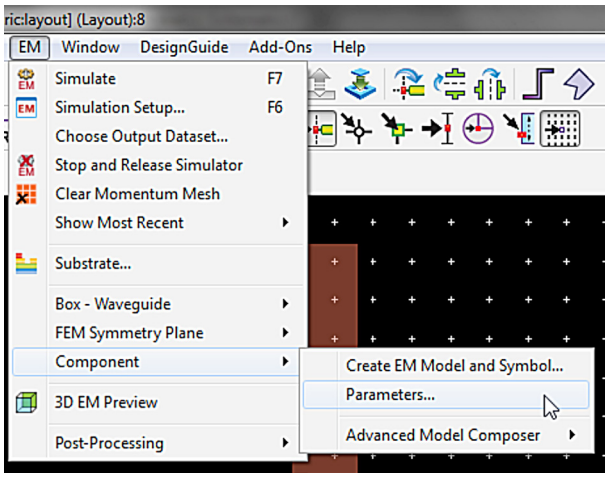


Figure 140.

In the parameter pop-up window, define 4 variables for capacitive and inductive lines and enter their nominal values alongwith the corresponding units and choose **Type = Subnetwork** as these parameters will be associated with Microstrip library components, which has parameterized artwork. If we are trying to parameterize the polygon/rectangle based components, then we can select the Nominal/Perturbed method which requires additional attention to the way components get parameterized.

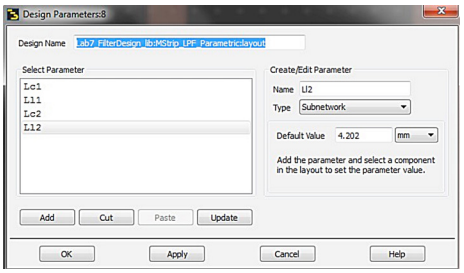


Figure 141.

Once the parameters have been added in the list, double-click the respective components and insert the corresponding variable names, please note that no units need to be defined here as we have already defined units in the variable parameter list. An example of one component has been shown below:

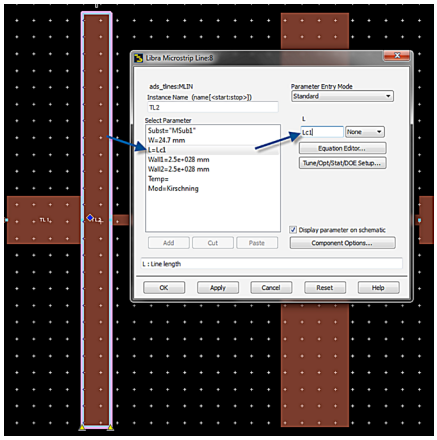


Figure 142.

After defining all the parameter values in the desired layout components we can create an EM model and symbol that can then be used for parametric EM cosimulation in the schematic. To create a parametric model and symbol for the layout, click the "**EM > Component > Create EM Model and Symbol**" option.

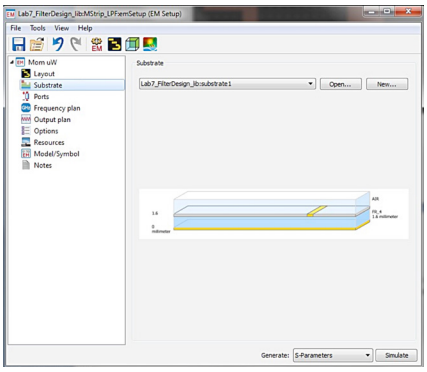


Figure 143.

Once done, observe the main ADS window where the name of the emmodel and symbol are displayed below the layout cell name as shown below:

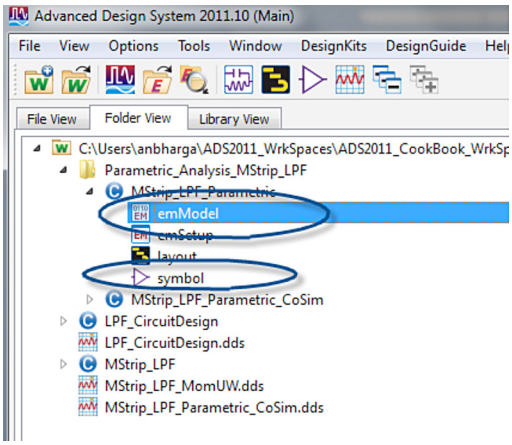


Figure 144.

Open a new schematic cell and drag and drop the emModel component to place it as subcircuit. You will notice the defined parameters being added to the emModel component, which can then be swept using the regular Parameter Sweep component in the ADS schematic as shown below. In this case, we have defined variables L1-L4 and assigned it to the emModel component. To start with, we sweep the length of L2 (1st inductive line) from 6.145 to 12.145 in steps of 1.

At this stage, we can decide to setup optimization and then optimize the layout component variables like any other circuit optimization, but please note that EM optimization will take longer as compared to circuit based optimization but produces more an accurate response as the EM simulation will be performed for every combination.

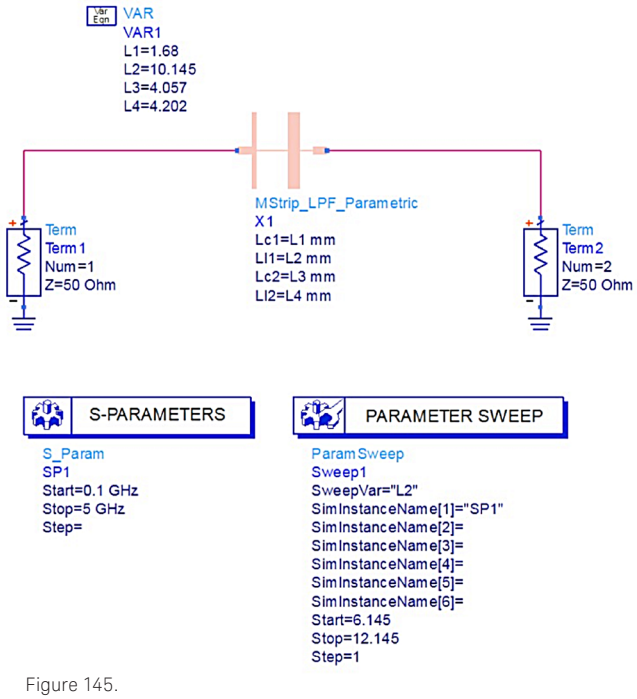


Figure 145.

Click the **Simulate** icon and plot the graph in the data display window to see how the filter response changes with the length of the 1st inductive line.

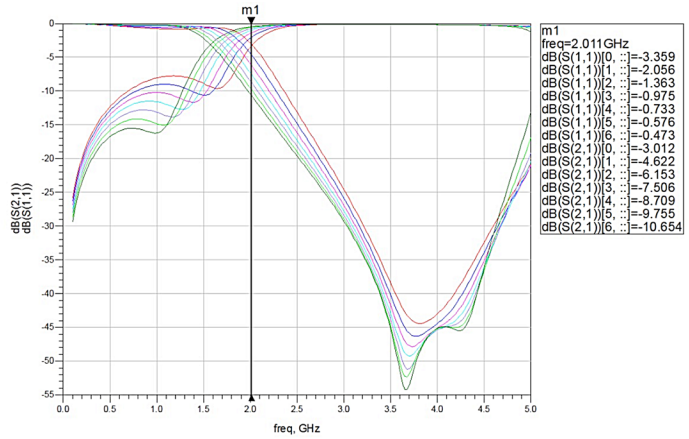


Figure 146.

From the data display, we can see that the 1st sweep value of L2 is providing a 3dB cutoff at *2 GHz* i.e. *L2=6.145 mm* seems to be the correct value.

Disable the parameter sweep and change the value of *L2 = 6.145 mm* and perform the simulation again to see the filter response. The circuit can be EM optimized if better return loss is expected from the circuit.

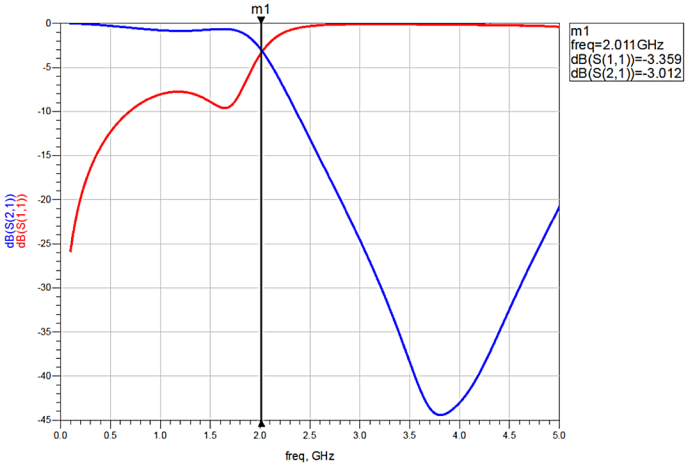


Figure 147.

Results and Observations

It is observed from the layout simulation that the Lowpass filter has a 3 dB cutoff frequency of 2 GHz after parametric EM analysis.

Simulation of a Lumped and Distributed Bandpass Filter Using ADS

Typical Design

Upper Cutoff Frequency (f_{c1})	: 1.9 GHz
Lower Cutoff Frequency (f_{c2})	: 2.1 GHz
Ripple in passband	: 0.5 dB
Order of the filter	: 3
Type of Approximation	: Chebyshev

Prototype Values of the Filter

The prototype values of the filter for a Chebyshev approximation is calculated using the formulae given above.

The prototype values for the given specifications of the filter are

g1 = 1.5963, g2 = 1.0967 & g3 = 1.5963

Lumped Model of the Filter

The Lumped values of the Bandpass filter after frequency and impedance scaling are given by:

$L'_1 = L_1 Z_0 / \omega_0 \Delta$

$C'_1 = \Delta / L_1 Z_0 \omega_0$

$L'_2 = \Delta Z_0 / \omega_0 C_2$

$C'_2 = C_2 / Z_0 \Delta \omega_0$

$L'_3 = L_3 Z_0 / \omega_0 \Delta$

$C'_3 = \Delta / L_3 Z_0 \omega_0$ where, Z_0 is 50Ω

$\Delta = (\omega_2 - \omega_1) / \omega_0$

The resulting lumped values are given by:

L'_1 = 63 nH

C'_1 = 0.1004 pF

L'2 = 0.365 nH

C'_2 = 17.34 pF

L'_3 = 63 nH

C'_3 = 0.1004 pF

The Geometry of the lumped element bandpass filter is shown in the next figure.

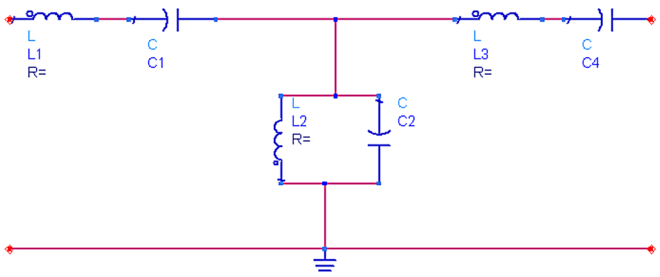


Figure 148.

Distributed Model of the Filter

Calculate the value of j from the prototype values as follows

$$\left[Z_0 \; j1 \; = \sqrt{\frac{\pi\Delta}{2\, g_1}} \right]$$

$$Z_0 \; j_n \; = \frac{\pi\Delta}{2\sqrt{g_n - 1}\, g_n} \qquad \text{For n =2, 3....N,}$$

$$Z_0 \; j_{N+1} \; = \sqrt{\frac{\pi\Delta}{2\, g_N \, g_{N+1}}}$$

Where, $\Delta = (\omega_2 - \omega_1) / \omega_0$

Z_0 = Characteristic Impedance = 50Ω

The values of odd and even mode impedances can be calculated as follows

$$z_{0e} = z_0[1 + jz_0 + (jz_0)^2]$$

$$z_{0o} = z_0[1 + jz_0 + (jz_0)^2]$$

Schematic Simulation Steps for the Lumped Bandpass Filter

Open the Schematic window of ADS and construct the lumped bandpass filter as shown below. Setup the S-Parameter simulation from 1 GHz to 3 GHz with steps of 5 MHz (401 points).

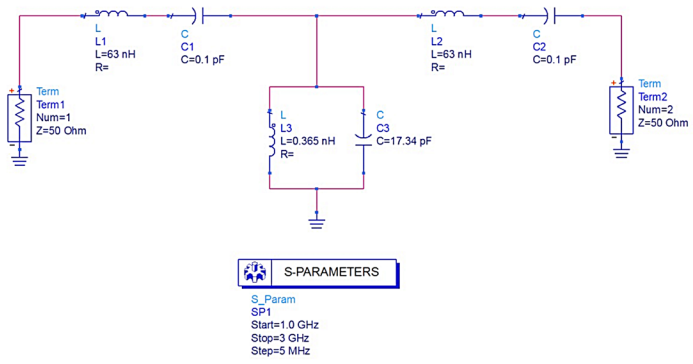


Figure 149.

Click the **Simulate** icon to observe the graph as illustrated:

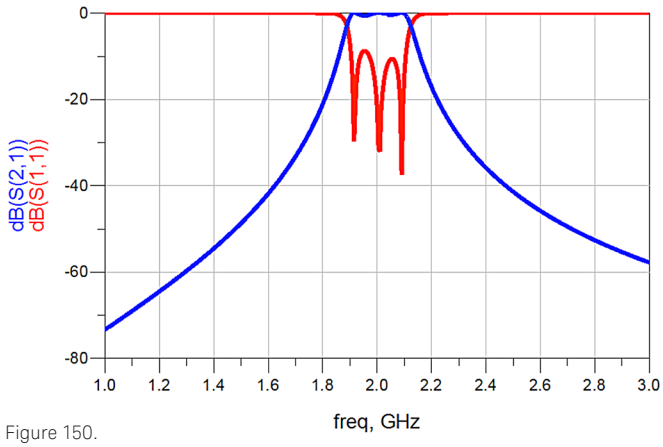


Figure 150.

Results and Observations

It is observed from the schematic simulation that the lumped model of the bandpass filter has an upper cutoff at 1.9 GHz, lower cutoff at 2.1 GHz and a roll off as per the specifications.

Layout Simulation Steps for the Distributed Bandpass Filter

Calculate the odd mode and even mode impedance values (Zoo & Zoe) of the bandpass filter using the design procedure given above. Synthesize the physical parameters (length & width) for the coupled lines for a substrate thickness of 1.6 mm and dielectric constant of 4.6.

The physical parameters of the coupled lines for the given values of Zoo and Zoe are given as follows:

Substrate Thickness : 1.6 mm

Dielectric Constant : 4.6

Frequency : 2 GHz

Electrical Length : 90 degrees

Section 1: Zoo = 36.23, Zoe = 66.65

Width = 2.545

Length = 20.52

Spacing = 0.409

Section 2: Zoo = 56.68, Zoe = 44.73

Width = 2.853

Length = 20.197

Spacing = 1.730

Section 3: Zoo = 56.68, Zoe = 44.73

Width = 2.853

Length = 20.197

Spacing = 1.730

Section 4: Zoo = 36.23, Zoe = 66.65

Width = 2.545

Length = 20.52

Spacing = 0.409

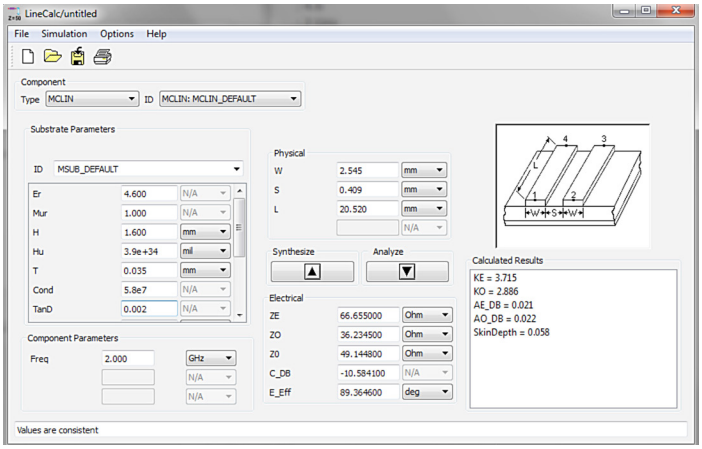


Figure 151.

Calculate the length and width of the 50 Ω line using the **linecalc** window of ADS as done earlier.

- 50 Ω Line:
- Width: 2.9 mm
- Length: 5 mm

Create a model of the bandpass filter in the layout window of ADS. The Model can be created by using the available library components or by drawing rectangles.

To create the model using library components select the MCFIL from TLines–Microstrip library. Select the appropriate kind of Microstrip line from the library and place it on the layout window as shown in Figure 152:

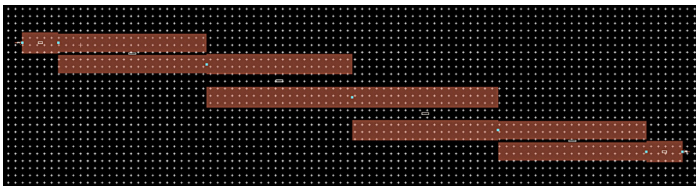


Figure 152.

Setup the EM simulation using the procedure defined earlier for 1.6mm FR4 dielectric and perform a Momentum simulation from 1 GHz to 3 GHz and don't forget to turn on Edge Mesh from **Options › Mesh** tab of the **EM Setup** window.

Once the simulation finishes, plot the S11 and S21 response of the BPF as shown below:

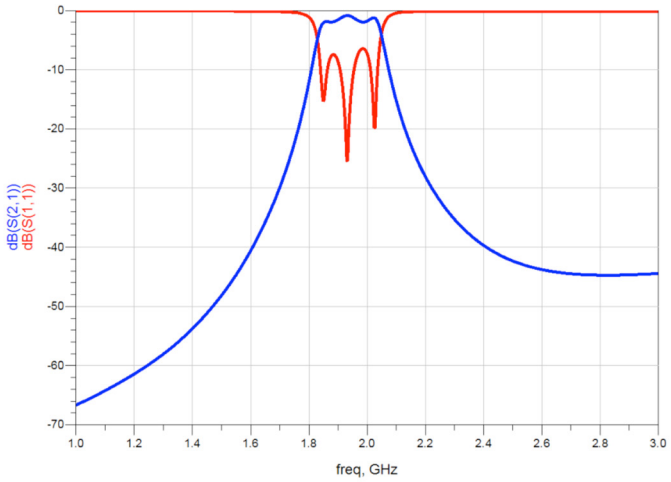


Figure 153.

Results and Observations

The results are good in the lumped element filter but the circuit needs to be simulated and probably needs to be re-optimized with the Vendor component libraries and we need to perform a Yield analysis simulation to take note of the performance variation, which may be caused due to tolerances of the lumped components.

For the distributed filter design, we can further optimize the design using the circuit simulator or Momentum EM simulator to obtain better bandpass filter characteristics, if desired, as the EM simulation is showing little degraded performance for fhs BPF.

Discrete and Microstrip Coupler Design

ADS Licenses Used: Linear Simulation, Momentum Simulation, Layout

Theory

A coupler is basically a device that couples the power from the input port to two or more output ports equally with less loss and with or without the phase difference. A branch line coupler is a 3 dB coupler with a 90°-phase difference between the two output ports. An ideal branch line coupler, as shown in Figure 154, is a four-port network and is perfectly matched at all four ports.

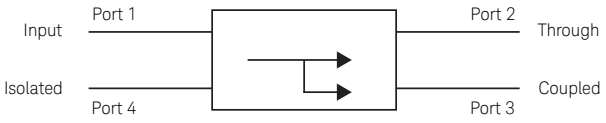


Figure 154.

The power entering port 1 is evenly divided between ports 2 and 3, with a phase shift of 90 degree between the ports. The 4th port is the isolated port and no power flows through it. The branch line coupler has a high degree of symmetry and allows any of the four ports to be used as the input port. The output ports are on the opposite side of the input port and the isolated port is on the same side of the input port. This symmetry is reflected in the S matrix as each row can be the transposition of the first row. The [S] matrix of the ideal branch line coupler is given as follows:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$

Figure 155.

The major advantage of this coupler is easier realization and the disadvantages are lesser bandwidth due to the use of a quarter wave length transmission line for realization and discontinuities occurring at the junction. To circumvent the above disadvantages, multi sections of the branch line coupler in cascade can increase the bandwidth by a decade and a 10° – 20° increase in length of the shunt arm can compensate for the power loss due to discontinuity effects.

Objective

Design a lumped element and distributed branch line coupler at 2 GHz and simulate the performance using ADS.

Design of Lumped Element Branch Line Coupler

Calculate the values of the capacitances (C_0 & C_1) and inductances (L) required for the Lumped model of the coupler shown below using the given formulae.

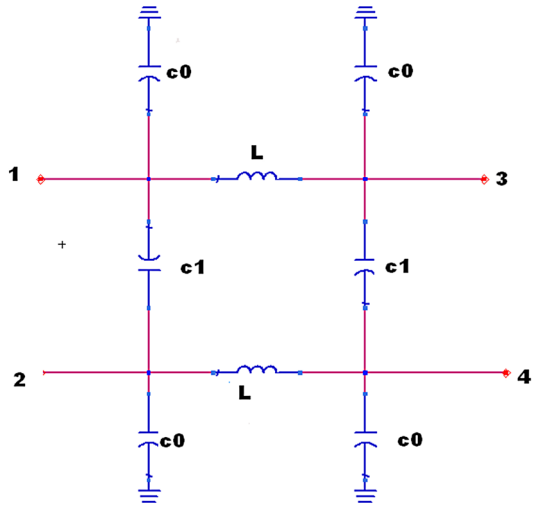


Figure 156.

$$\omega = 2\,\pi\,f_c$$

$$C_1 = \frac{1}{\omega Z_0 \sqrt{K}} \quad \text{Where K = 1 for the 3dB coupler}$$

$$C_0 \frac{1}{(\omega^2 L)} C_1$$

$$L = \frac{Z_0}{\omega \sqrt{1 + Z_o \omega C_1}}$$

Where,

- f_c is the design frequency of the coupler
- Z_0 is the characteristic impedance of the transmission line

Typical Design Specs

Design Frequency f_c = 2 GHz

Angular Frequency ω in radians = $2\pi f_c$ = 1.25×10^{10}

Characteristic Impedance Z_0 = 50 Ω

By substituting the values in the above design equation, the values for the lumped model are obtained as follows:

C_1 = 1.6 pF

L = 2.8 nH

C_0 = 0.66 pF

Schematic Simulation Steps

1. Open the **Schematic** window of ADS
2. From the lumped components library select the appropriate components necessary for the lumped model. Click the necessary components and place them on the schematic window of ADS as shown in next figure.
3. Setup an S-Parameter simulation for 1.5 GHz to 2.5 GHz with 101 points and run the simulation.

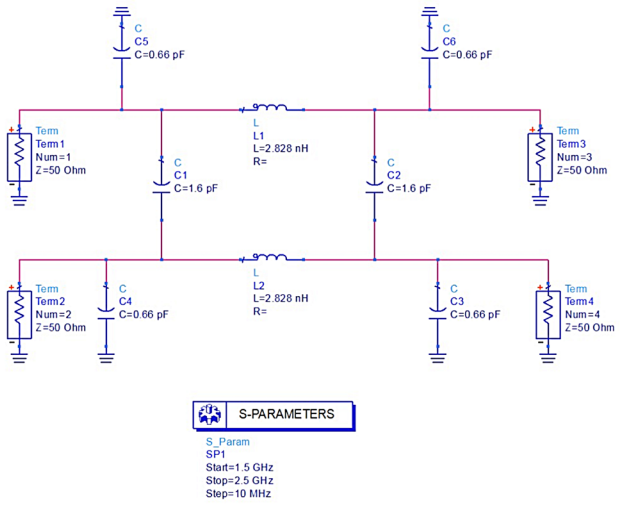


Figure 157.

4. Once the simulation is finished plot the required graphs to observe the Coupler response as shown in the figure below.

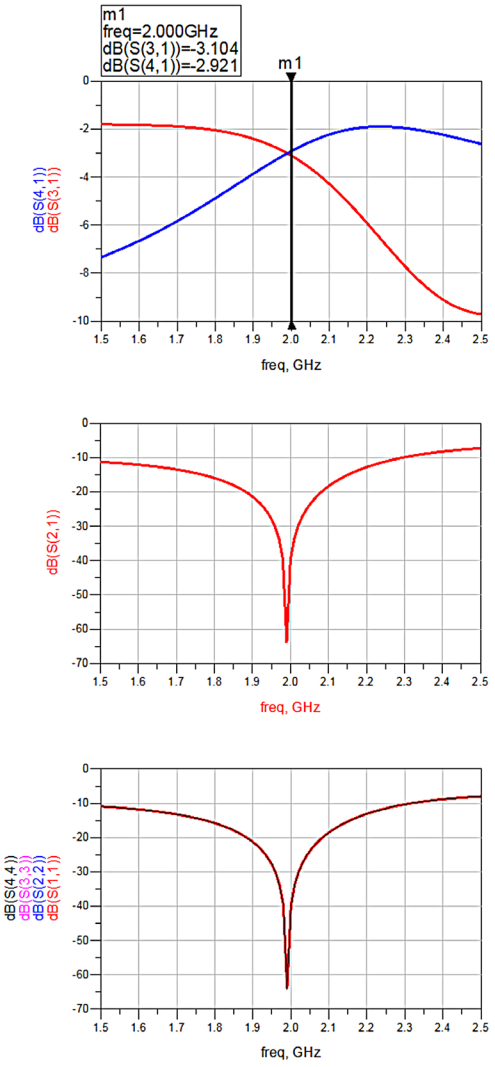


Figure 158.

Design of a Distributed Branch Line Coupler

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the coupler. For the present example, we will select following dielectric parameters:
   a. Er = 4.6
   b. Height = 1.6 mm
   c. Loss Tangent = 0.0023
   d. Metal Thickness = 0.035 mm
   e. Metal Conductivity = 5.8E7 S/m
2. Calculate the wavelength λ_g from the given frequency specifications as follows:

$$\lambda_g = \frac{C}{\sqrt{\varepsilon_r}\, f}$$

Where, c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate.

3. Synthesize the physical parameters (length & width) for the λ/4 lines with impedances of Z_0 and $Z_0/\sqrt{2}$ (Z_0 is the characteristic impedance of the microstrip line which is taken as 50Ω). The geometry of the Branch line coupler is shown in the figure below.

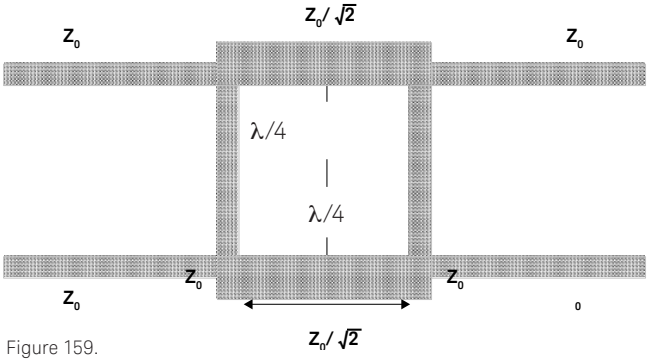


Figure 159.

Layout Simulation Using ADS

1. Calculate the physical parameters of the branch line coupler from the electrical parameters like Z_0 and electrical length using the above given design procedure. The physical parameters can be synthesized using Linecalc as described in earlier labs. The physical parameters of the microstrip line for the 50Ω (Z_0) and 35Ω ($Z_0/\sqrt{2}$) are as follows:

   50Ω Line:
   - i. Width - 2.9 mm
   - ii. Length – 20 mm

   35Ω Line:
   - iii. Width - 5.14 mm
   - iv. Length – 19.5 mm

2. Create a model of the branch line coupler in the layout window of ADS. The Model can be created by using the available Microstrip library components or by drawing rectangles.

3. To create the model using library components, select the TLines – Microstrip library. Select the appropriate kind of Microstrip line from the library and place it on the layout window as shown in the figure below. We need to add a Microstrip TEE at the 4 junctions for proper connections of the lines as highlighted in the figure below.

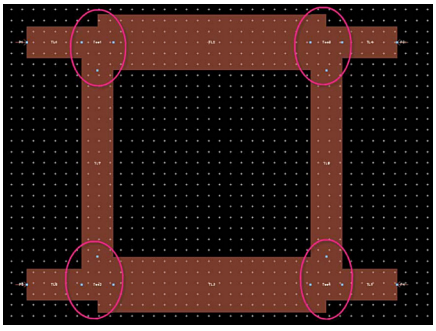


Figure 160.

4. Using the EM setup window, define the dielectric and conductor properties using the procedure described in the Momentum simulation lab. Once defined properly, it should look as shown below

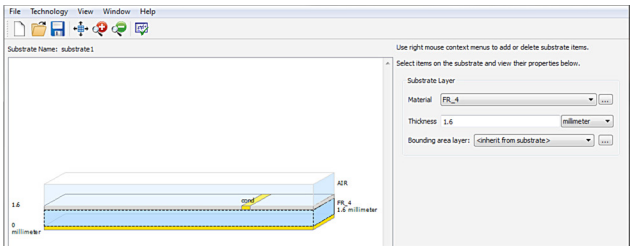


Figure 161.

5. Setup the simulation frequency from 1.5GHz – 2.5 GHz, turn on Edge Mesh from the **Options > Mesh** tab of the EM setup window and click the **Simulate** button.

6. Once the simulation is finished, plot and observe the required response and note that the frequency is shifted to the lower side as illustrated.

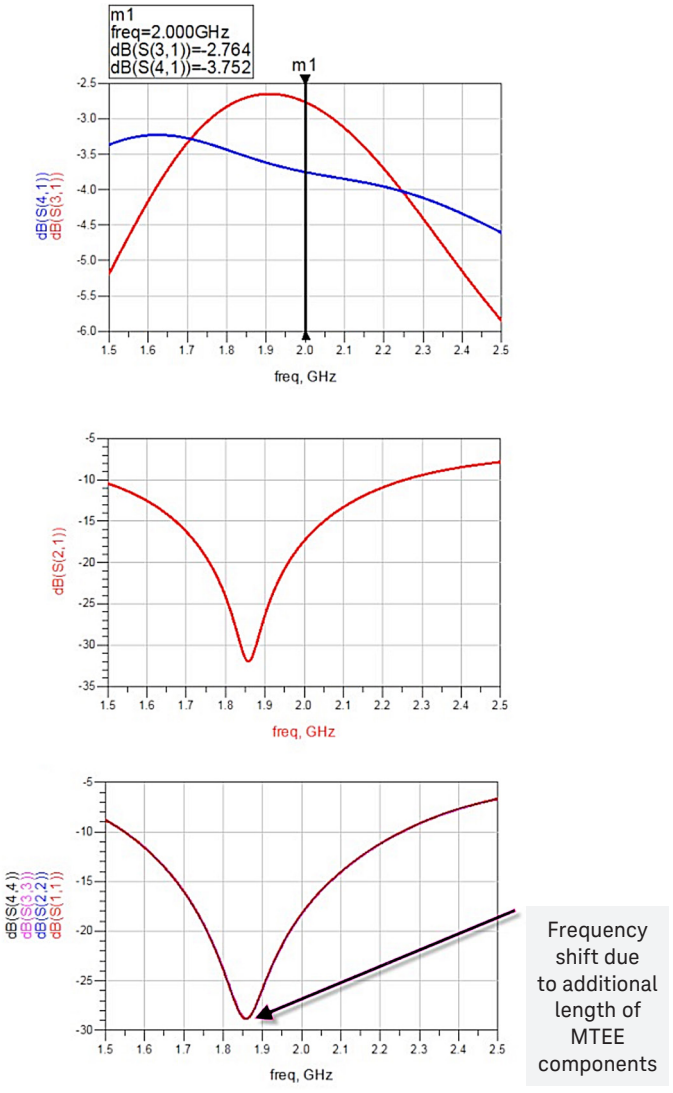


Figure 162.

7. In order to compensate for the TEE effect, we need to reduce the calculated lengths of the coupler lines by ~ w/2 of the intersecting line, e.g. *19.5 mm 35Ohm* line should have approx. length of *18.2 mm and 19.5 mm*, *50Ohm* vertical line should have length of 17.1 mm.

8. Modify the length of lines and reconnect the lines as shown below and simulate the layout again with the same simulation setting to observe the response coming close to the desired *2 GHz* frequency.

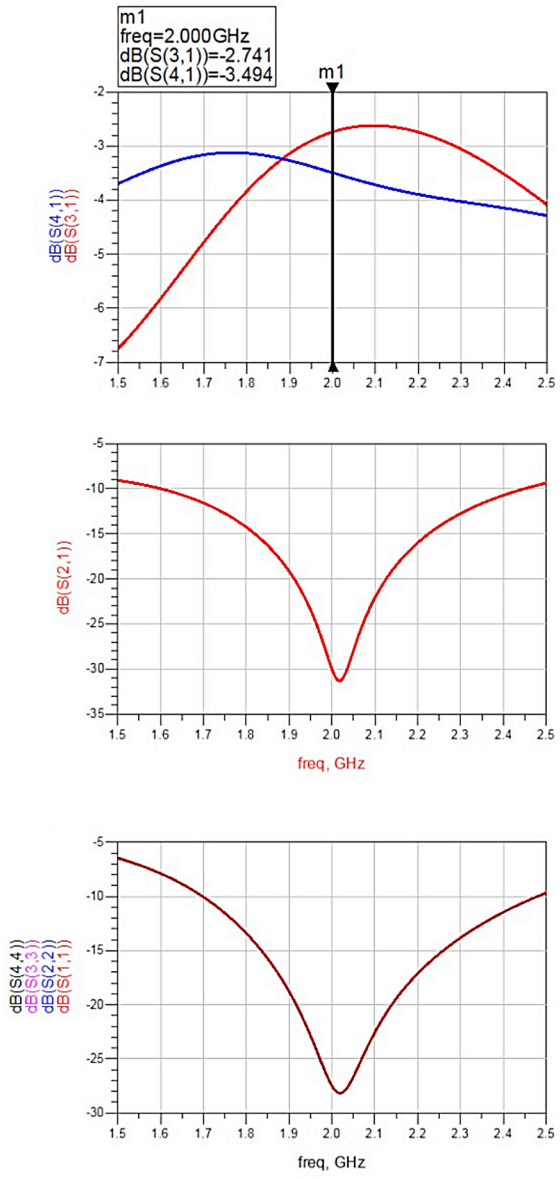


Figure 163.

Conclusion

The results are good in the lumped element coupler, but the circuit needs to be simulated and probably needs to be re-optimized with the Vendor components libraries and we need to perform a Yield analysis simulation to take note of the performance variation, which may be caused due to tolerances of the lumped components.

For the distributed coupler design, we can optimize the design using the circuit simulator or Momentum EM simulator to obtain better coupling, if desired, as the circuit is showing over-coupling in one of the branches.

Microstrip and CPW Power Divider Design

ADS Licenses Used: Linear Simulation, Momentum (EM) Simulation, Layout

Theory

A power divider is a three-port microwave device that is used for power division or power combining. In an ideal power divider the power given in port 1 is equally split between the two output ports for power division and vice versa for power combining as shown below. Power divider finds applications in coherent power splitting of local oscillator power, antenna feedback network of phased array radars, external leveling and radio measurements, power combining of multiple input signals and power combining of high power amplifiers.

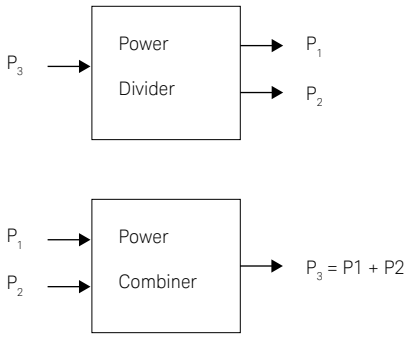


Figure 164.

T–Junction Power Divider

The different types of power dividers are a T-Junction power divider, a Resistive divider and a Wilkinson power and hybrid coupler. The T-Junction power divider is a simple 3-port network and can be implemented in any kind of transmission medium like microstrip, stripline, coplanar wave guide etc. Since, any 3-port network cannot be lossless, reciprocal and matched at all the ports, the T-Junction power divider being lossless and reciprocal cannot be perfectly matched at all the ports. The T-Junction power divider can be modeled as a junction of three transmission lines as shown in the figure below.

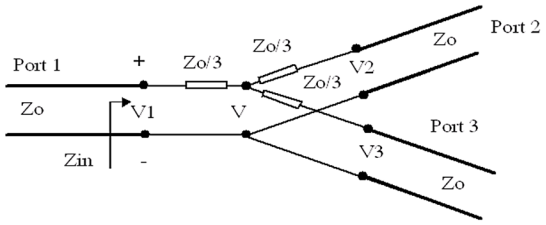


Figure 165.

Objective

To design various types of Power Dividers at 3 GHz and simulate the performance using ADS.

Design of Distributed T-Junction Power Divider

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the power divider.
2. Calculate the wavelength λ_g from the given frequency specifications as follows:

$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r}\, f}$$

Where, c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate

3. Synthesize the physical parameters (length & width) for the $\lambda/4$ lines with impedances of Z_0 and $\sqrt{2}\, Z_0$ (Z_0 is the characteristic impedance of microstrip line which is = 50Ω)

Layout Simulation Using ADS

1. Calculate the physical parameters of the T-Junction power divider from the electrical parameters like Z_0 and electrical length using the above given design procedure. The physical parameters can be synthesized using Linecalc. The Physical parameters of the microstrip line for the 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\, Z_0$) are as follows

2. Dielectric properties: Er = 4.6, Height = 1.6 mm, Loss Tangent = 0.0023, Metal Height = 0.035 mm, Metal Conductivity = 5.8E7.

   50Ω Line:

   Width – 2.9 mm

   Length – 13.3 mm

   70.7Ω Line:

   Width – 1.5 mm

   Length – 13.6 mm

3. Create a model of the T-Junction power divider in the layout window of ADS. The Model can be created by using the available Microstrip library components or by drawing rectangles.

4. To create the model using library components, select the TLines – Microstrip library. Select the appropriate Microstrip line from the library and place it on the layout window as shown in the next figure.

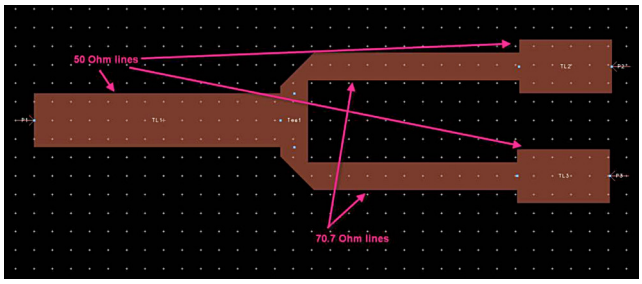


Figure 166.

– Connect the Pins and input and output terminals and set the EM simulation as described in the EM simulation chapter earlier. Once done, it should be as in the figure below.

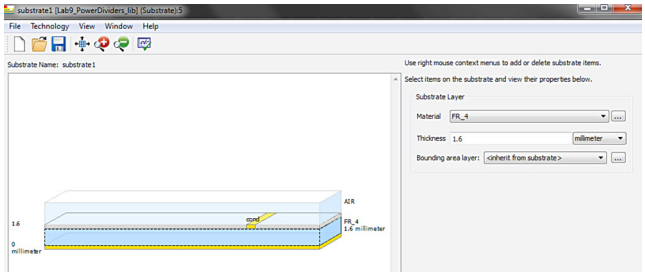


Figure 167.

– Define the simulation frequency from 2 GHz – 3 GHz and turn on Edge Mesh from the **Options > Mesh** tab in the EM set up window.

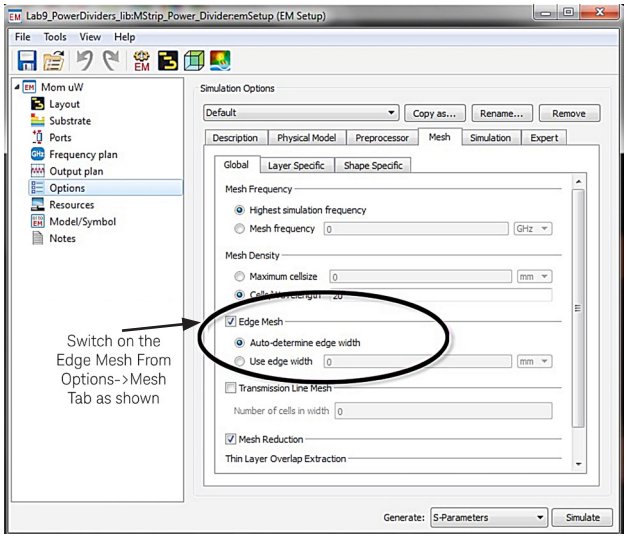


Figure 168.

– Click the **Simulate** icon and plot the results to observe the T-Junction power divider response as shown below.

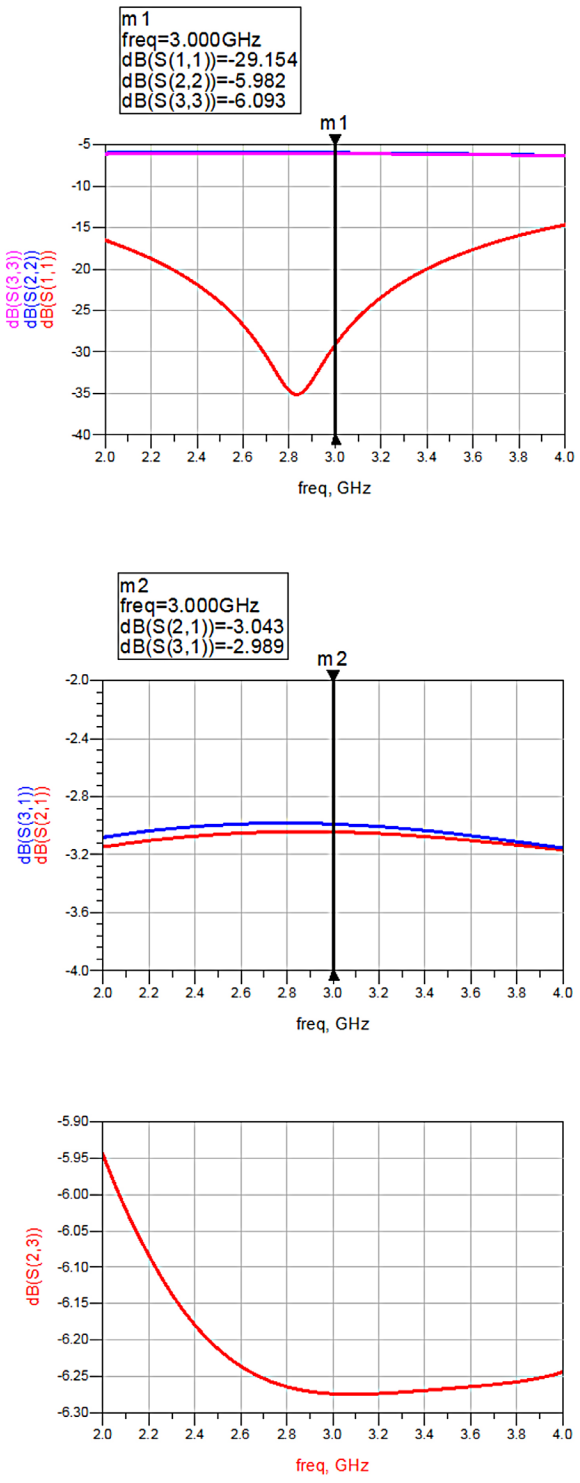


Figure 169.

Results and Observations

It is observed from the layout simulation that the T-Junction power divider has an insertion loss (S_{12} and S_{13}) of 3.0dB and return loss (S_{11}) of about 29 dB but as expected isolation between 2 output branches is only 6 dB representing real characteristics of T-Junction power divider.

Wilkinson Power Divider

The Wilkinson power divider is a robust power divider with all the output ports matched and only the reflected power is dissipated. The Wilkinson power divider provides better isolation between the output ports when compared to the T-Junction power divider The Wilkinson power divider can also be used to provide arbitrary power division. The geometry of a Wilkinson power divider and its transmission line equivalent is shown in the figure below.

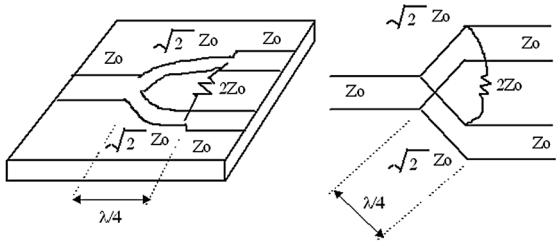


Figure 170.

Design of a Lumped Model Wilkinson Power Divider

Calculate the values of the capacitances (C_1 & C_2), inductances (L_1, L_2 & L_3) and resistance (R1) required for the Lumped model of the coupler shown in the illustration below using the given formulae.

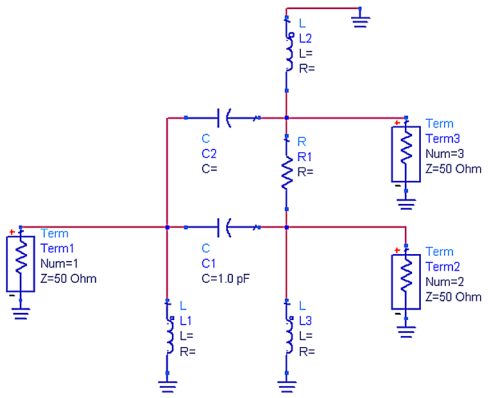


Figure 171.

$$C_1 = C_2 = \frac{1}{\sqrt{\left(2R_a \cdot \sqrt{R_b R_c} \cdot \omega^2\right)}}$$

$$L_3 = L_2 = \sqrt{\frac{2R_a\sqrt{R_b R_c}}{\omega^2}}$$

$$L_1 = \sqrt{\frac{R_a\sqrt{R_b R_c}}{2\omega^2}}$$

$$R = 2\sqrt{R_a R_b}$$

Where, for any arbitrary impedance $Z_0 = R_a = R_b = R_c = 50$ohms

ω is the angular frequency

Typical Design

Design frequency = 3 GHz

Angular frequency in radians = 1.88×10^{10}

$C_1 = C_2 = 0.75$ pF,

$L_2 = L_3 = 3.75$ nH

$L_1 = 1.87$ nH

R = 100 Ω

Schematic Simulation Steps

1. Open the Schematic window
2. From the lumped components library, select the appropriate components necessary for the lumped model. Click the necessary components and place them on the schematic window as shown in the figure below.

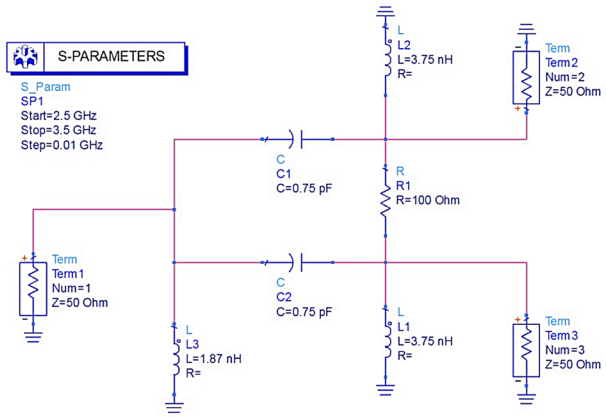
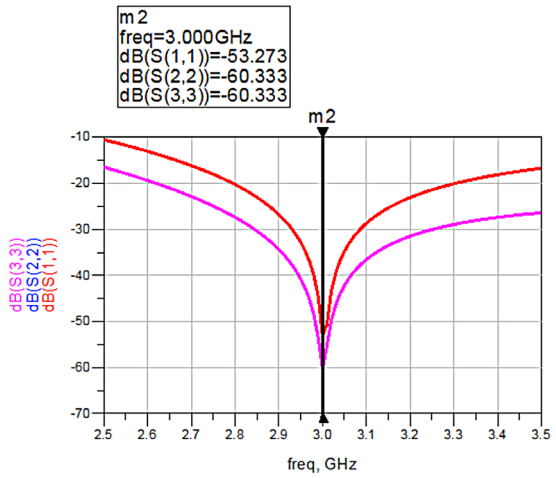


Figure 172.

3. Setup the S-Parameter simulation from 2.5 GHz – 3.5 GHz with a step size of 0.01 GHz. Perform the simulation and observe the parameter response as shown below.



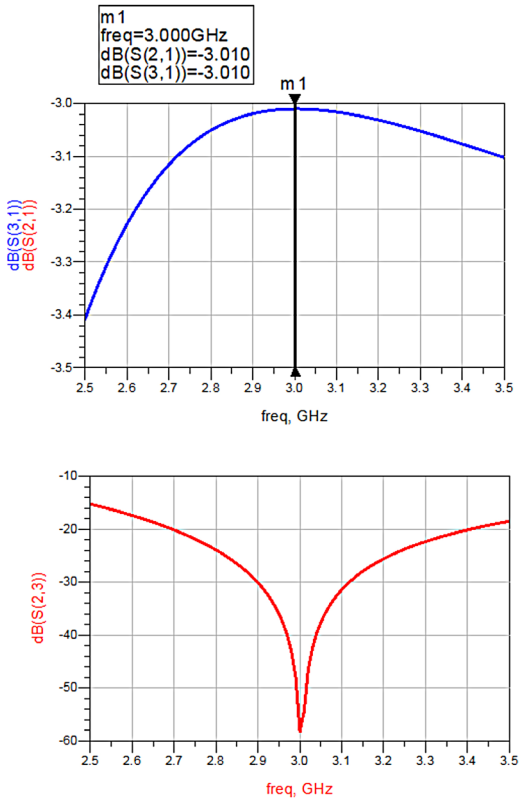


Figure 173.

Results and Observations

It is observed from the schematic simulation that the lumped model of the Wilkinson power divider has an insertion loss (S_{12} and S_{13}) of 3 dB and return loss (S_{11}) of <30 dB.

Design of Distributed Wilkinson Power Divider

Layout Simulation Using ADS

1. Calculate the physical parameters of the Wilkinson power divider from the electrical parameters like Z_0 and electrical length similar to T-Junction power divider. The physical parameters can be synthesized using Linecalc. The physical parameters of the microstrip line for the 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\,Z_0$) are as follows on the dielectric selected in the in the T-Junction power divider design.

50Ω Line:

Width – 2.9 mm

Length – 13.3 mm

70.7Ω Line:

Width – 1.5 mm

Length – 13.6 mm

2. The layout of the Wilkinson power divider will be done the same as we did earlier except for the fact that we will use an isolation resistor of 2*Z0, which in our case will be 100Ohm since the characteristic impedance is 50 Ohm.
3. Use TLines-Microstrip components or the rectangle/polygon icon to create the power divider structure. Please note that in the Wilkinson power divider, we will need 2 extra Pins at the place where we shall later connect a 100 Ohm resistor.

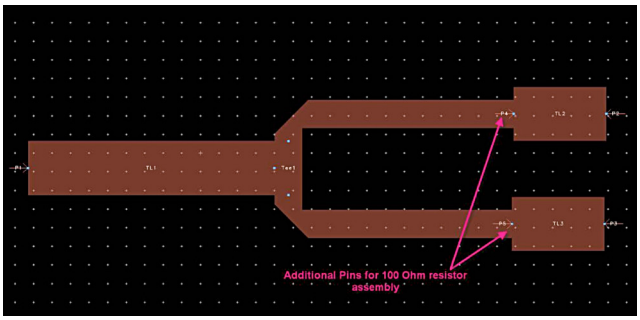


Figure 174.

4. Define a new or reuse the substrate defined earlier in the T-Junction power divider exercise. Define the frequency sweep from 2.5 GHz – 3.5 GHz and from the Model/Symbol option in the EM setup window, click the **Create Now** button under the EM Model and Symbol fields to generate an EM Model data container and layout look-alike symbol so that we can use this layout component to perform resistor assembly and EM cosimulation. Detailed steps for this are provided in the EM simulation section.

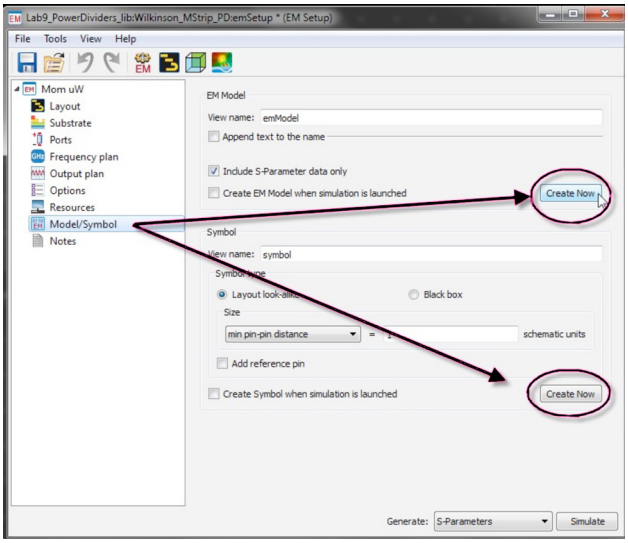


Figure 175.

5. Open a new schematic cell, drag & drop this layout on the same and connect Terminations and Resistor as shown below. Set up a S-Parameter simulation from 2.5 GHz – 3.5 GHz with Step=0.01 GHz

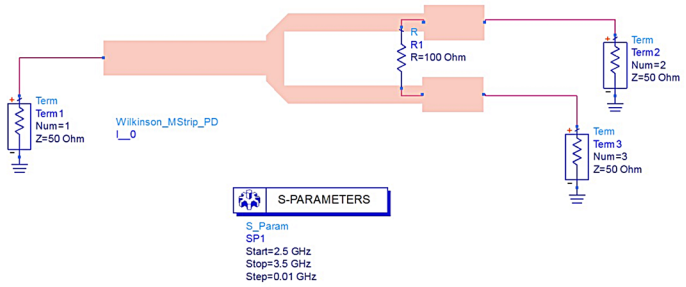


Figure 176.

6. Click the **Simulate** icon, then plot the graphs in the data display as shown below.

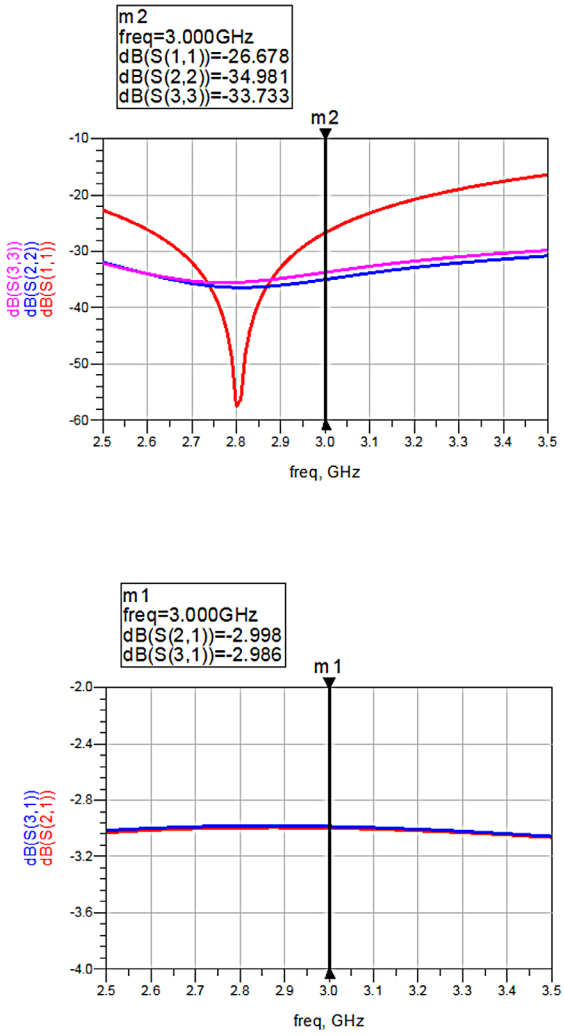


Figure 177.

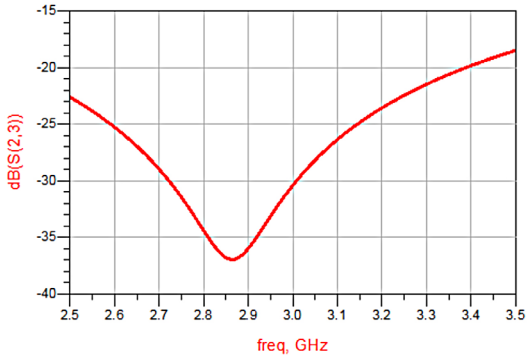


Figure 178.

Results and Observations

It is observed from the layout simulation that the Wilkinson power divider has an insertion loss (S_{12} and S_{13}) of 3.0dB and return losses (S_{11}, S_{22}, S_{33}) < -25 dB.

Design of CPW T-Junction Power Divider

Objective

To design a CPW T-Junction power divider at 2.4 GHz and simulate the performance using ADS.

Design Procedure

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the power divider.
2. Calculate the wavelength λ_g from the given frequency specifications as follows:

$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r}\, f}$$

Where, c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate

3. Synthesize the physical parameters (length & width) for the $\lambda/4$ CPW line with impedances of Z_0 and $\sqrt{2}\, Z_0$ (Z_0 is the characteristic impedance of CPW line = 50Ω).

Layout Simulation Using ADS

1. Calculate the physical parameters of the T-Junction power divider from the electrical parameters, like Z_0, and electrical length using the above design procedure. The physical parameters can be synthesized using Linecalc as shown in the following illustration. The Physical parameters of the CPW line for 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\, Z_0$) are as follows:

50Ω Line:

Width:	3 mm
Length:	20 mm
Gap:	0.37mm

70.7Ω Line:

Width:	1.5 mm
Length:	19.6 mm
Gap:	0.69 mm

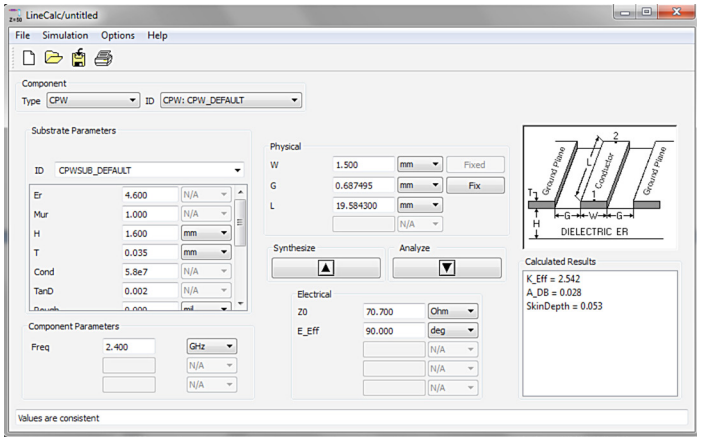


Figure 179.

2. Create a model of the T-Junction power divider in the layout window of ADS. The Model can be created by using the available TLines-Waveguide library components or by drawing rectangles.

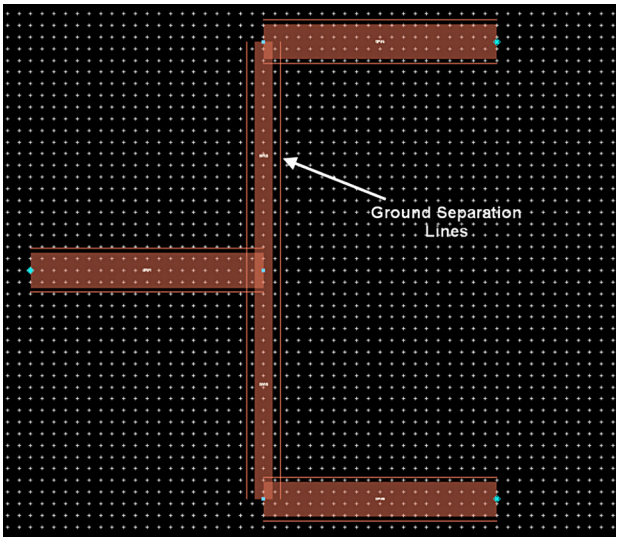


Figure 180.

The ground separation lines will help us as a guiding line for ground creation and we can simply use the rectangle icon to create the ground for these CPW lines as shown below.

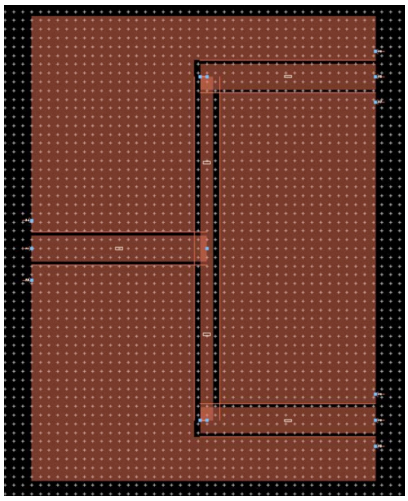


Figure 181.

3. Assign Pins in layout for the CPW transmission line by clicking the Pin icon and placing them in the circuit i.e. 1 Port on the main line and placing 2 ports attached to the ground fill on either side of the main signal pin. For the present case, we shall have a total of 9 Pins, i.e. 3 Signal Pins and 6 ground pins. For easy remembrance, place 3 signal pins so that they are named as P1, P2 & P3 and then start placing P4 & P5 around P1, P6 & P7 around P2 and P8 & P9 around P3. **It is strongly advised to place ground ports slightly inside the ground pattern**.

4. Defining the CPW substrate without the ground at the bottom will require the substrate to be defined differently than what we have done so far. Open the EM setup window, define the required dielectric as described in earlier labs and do the following additional actions:
   a. Right-click the FR4 and select Insert Substrate Layer Below. Right-click the Cover and select Delete Cover.
   b. Change the bottom side dielectric to be AIR (which is by default provided in the substrate definition window). Once done, it should look as shown below.

Figure 182.

5. Go to the **Ports** option in the EM setup window and select Ports 4 – 9, right-click and delete so that they are removed from the list and appear at the bottom side.

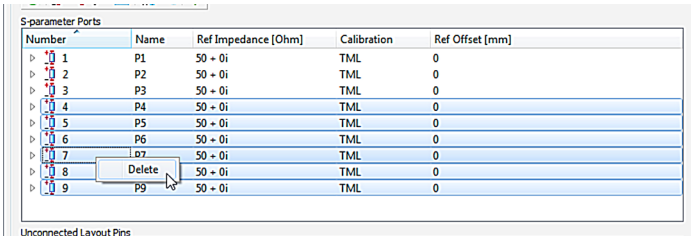


Figure 183.

6. From the Unconnected Layout Pins, drag and drop P4 and P5, which are placed on either side of P1 in the layout on –GND so that it looks as below. Do this also for P2 and P3 using the respective unconnected Layout Pins.

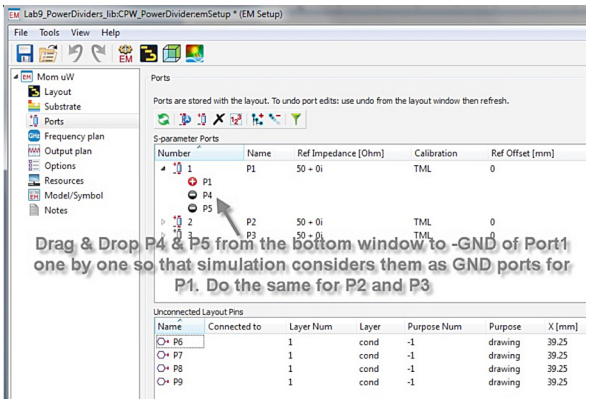


Figure 184.

7. Once done, Port assignment will be as shown below.

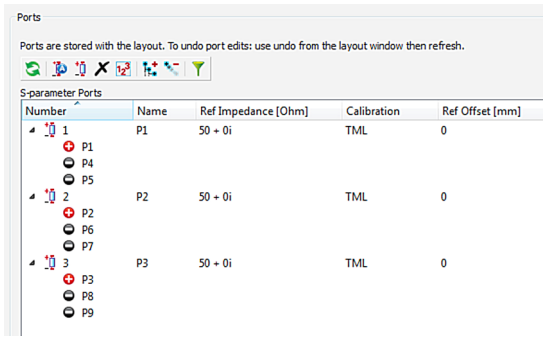


Figure 185.

8. Setup simulation frequency as 2 GHz- 2.8 GHz and turn on Edge Mesh from the **Options > Mesh** option of the **EM Setup** window. Perform simulation and plot the desired response to observe the Simulation Results as shown below m1 freq=2.400GHz dB(S(1,1))=-20.244 dB(S{2,1))=-3.784 dB(S{3,1))=-3.446

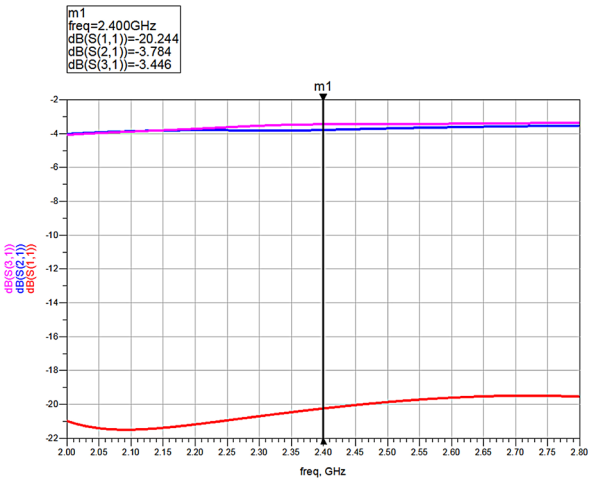


Figure 186.

Microwave Amplifier Design

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ADS Licenses Used: Linear Simulation

Abstract

The purpose of this paper is to help designers understand a simple procedure to design and develop Amplifiers. There are many text books available on Amplifier theory and design but they often leave a gap between theory and practical considerations that should be understood by a designer to produce a good amplifier circuit that compares well with simulated data so that minimal or almost no post production tuning is required for the Amplifier. This paper tries to collect basic theory of Amplifier design as well as the practical procedure that needs to be adopted for making designs right the first time to save designers time and efforts. This paper focuses more on CAD aided design procedures to design amplifiers because CAD software has become a necessity for a design house to design accurately and shorten time to market. The design process utilized in this paper makes use of Keysight Advanced Design System (ADS) software.

Introduction

Amplifiers are an integral part of any communication system. The purpose of having an amplifier in a system is to boost the signal to the desired level. It also helps in keeping the signal well above noise so that it can be analyzed easily and accurately. The choice of amplifier topology is dependent on the individual system requirements and can be designed for Low Frequency applications, medium to high frequency applications, mm-wave applications etc. Depending upon the system in which they are used, amplifiers can adopt many design topologies and can be used at different stages of the system and accordingly they are classified as Low Noise Amplifiers, Medium Power Amplifiers, and Power Amplifiers etc. The most common structure that still finds application in many systems tends to be a Hybrid MIC amplifier. The main design concepts for amplifiers regardless of frequency and system remain the same and need to be understood very clearly by designers. Specific frequency ranges pose their own unique design challenges and need to be taken care of appropriately. This paper focuses on the design of a small signal C-band Hybrid MIC amplifier. This procedure is equally valid for other amplifiers operating in other frequency ranges with minor changes in the design procedure.

Amplifier Theory

There are a few things that need to be understood before starting an amplifier design, like stability and matching conditions. These are discussed below. There are many references available on amplifier basic concept and design procedures, the formula presented in this paper are taken from one of them [1]:

Stability Condition

Stability analysis is the first step in any amplifier design. The stability of an amplifier or its resistance to oscillation is an important consideration in a design and can be determined from S-parameters, the matching networks, and the terminations. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance [1]. This occurs when $|\Gamma_{IN}| > 1$or $|\Gamma_{OUT}| > 1$, which for a unilateral device occurs when $|S_{11}| > 1$ or $|S_{22}| > 1$.

Unconditional stability of the circuit is the goal of the amplifier designer. Unconditional stability means that with any passive load presented to the input or output of the device, the circuit should not become unstable, i.e. it will not oscillate. In general, for a linear 2-port device characterized by S-parameters, the two necessary and sufficient conditions to guarantee unconditional stability are a) K >1 and b) |Δ|< 1, where

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

$$K = (1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2) / (2\,|S_{21}\,S_{12}|)$$

Matching Conditions

An amplifier could be matched for a variety of conditions like Low Noise applications, the unilateral and bilateral case. The formulae for each condition are given below [1].

Optimum Noise Match

The matching for lowest possible noise figure over a band of frequencies requires that a particular source impedance be presented to the input of the transistor. The noise-optimizing source impedance is called Γ_{opt}, and is obtained from the manufacturers data sheet. The corresponding load impedance is obtained from the cascade load impedance formula.

$$\Gamma_L = \left(\frac{S_{22} - \Gamma_{opt}\Delta}{1 - \Gamma_{opt}S_{11}}\right)^*$$

Unilateral Case

$$\Gamma_{IN} = S_{11} + \left(\frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\,\Gamma_L}\right)$$

$$\Gamma_{OUT} = S_{22} + \left(\frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\,\Gamma_S}\right)$$

Bilateral Case (when $S_{12} \neq 0$)

$$\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^{\,2} - 4|C_1|^2}}{2C_1}$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^{\,2} - 4|C_2|^2}}{2C_2}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

The common source configuration is normally chosen for the highest gain per stage. If the stability factor K>1, the network gives MAG. If K<1, the network could cause oscillations, i.e. Gmax is infinite and given as

$$G_{max} = \frac{S_{21}}{S_{12}}\left(k - \sqrt{(k^2 - 1)}\right)$$

This should be avoided by locating the region of instability in the Γ_S and Γ_L planes.

CAD Oriented Design Procedure

The CAD oriented design procedure consists of the following steps.

1. DC Analysis
2. Bias circuit design
3. Stability analysis
4. nput and Output matching network design
5. Overall Amplifier performance optimization

Amplifier Specifications

- Frequency Band: 5.3 GHz – 5.5 GHz
- Gain: 12 dB or more
- Gain Flatness: +/- 0.25 dB (max.)
- Input/Output Return Loss: < -15 dB
- DC Power Consumption: 50 mW (max.)

DC Analysis

Based on the frequency range and the gain requirement, the CFY67-08 HEMT device was selected for the amplifier design. The first analysis that needs to be performed is the DC analysis to find out the right bias points for the amplifier. The following figure shows the DC analysis setup and Figure 188 shows the DC analysis results for the same. Based on the DC Power consumption and Gm requirement, bias points are selected as Vgs=-0.1V and Vds=3V. *To get the DC IV sweep setup shown below, please click* ***Insert > Template > FET Curve Tracer***, insert the active device (FET) and connect the proper wires and modify the Sweep parameters as per the device selected.

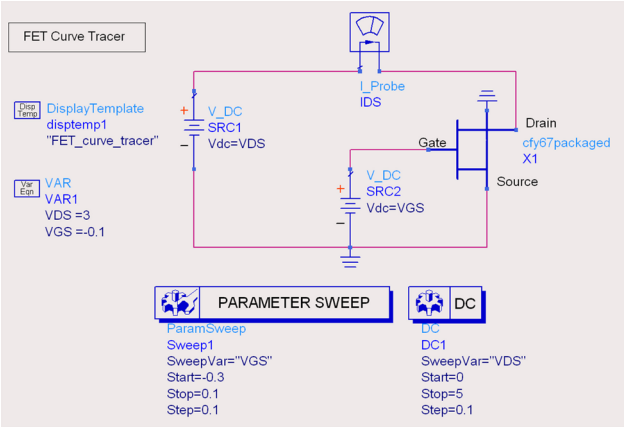


Figure 187.

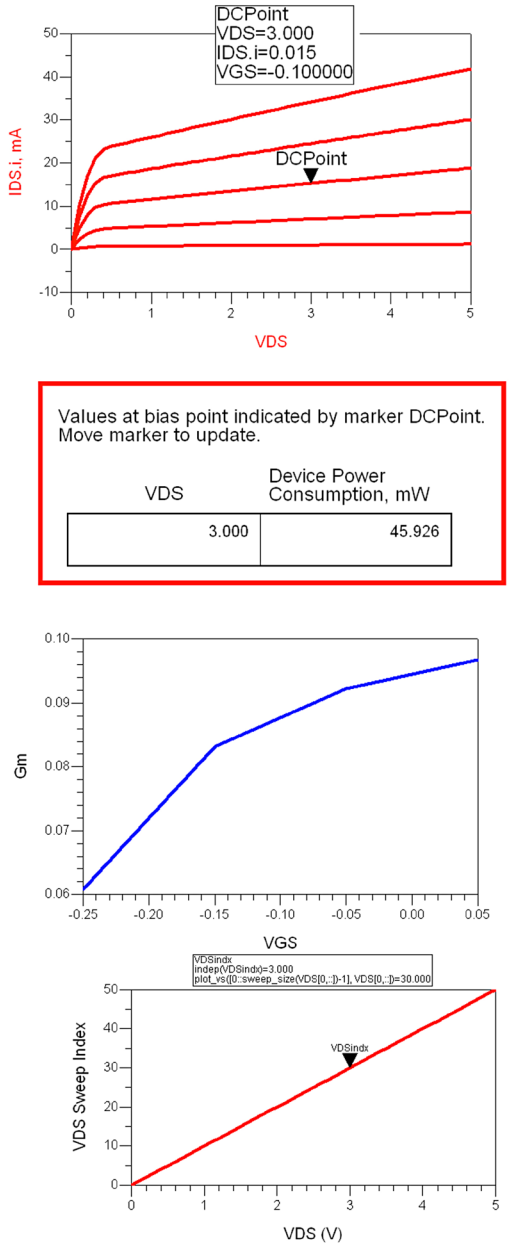


Figure 188.

Bias Network Design

Bias network design for amplifiers is dependent on the frequency range in which the amplifier needs to be designed, that is to say if the amplifier needs to be designed for a low frequency application, then a choke (inductor) is used. However, getting discrete inductors at microwave frequencies is difficult, so a high-impedance quarter wavelength line (λ/4) at the center frequency is the best possible choice for the bias network design. The thing that needs to be noted in bias circuit design is that more often than not this λ/4 is followed by a resistor or a bypass capacitor and these components add extra length to the λ/4 line, which designers sometimes neglect and this could cause some desired RF frequency power to be dissipated in this branch. This affects the gain and frequency response of the amplifier, so this calculated λ/4 line needs to adjusted by taking proper care regarding these extra elements and their footprints. One commonly used method is to use a Radial stub immediately after the λ/4 high-impedance bias line. This will help to achieve proper isolation at the desired RF frequency, no matter what component is added after the λ/4 long bias line.

The schematic illustration below shows the circuit design for a bias circuit where it can be seen that the high-impedance λ/4 bias line is immediately followed by a Radial stub and then by a resistor and capacitor to ground. For clarity, the layout of the bias network is shown.

The following illustration shows the results for the bias circuit. It can be seen that this design is acting as a near perfect bias network between 5.3 GHz – 5.5 GHz.

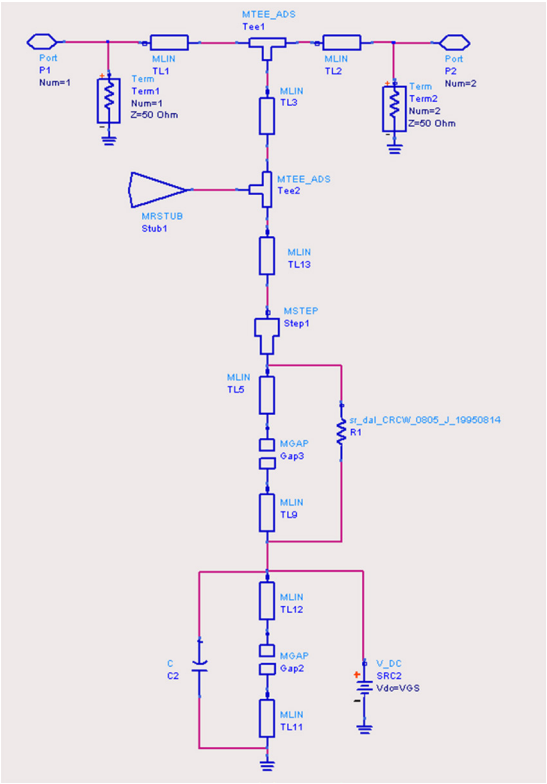


Figure 189.

Figure 190.

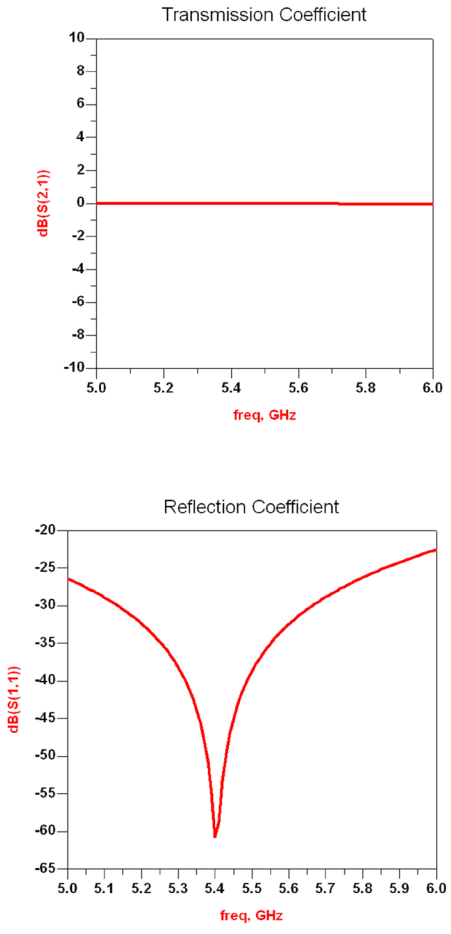


Figure 191.

Stability Analysis

Stability analysis is a very important aspect of any active circuit design and is equally important in Amplifier design. The illustration below shows the circuit that was obtained after adding input and output bias networks. Insert the StabFact component from the Palette Simulation – S_Parameter to calculate the Stability Factor for the amplifier circuit as shown below.

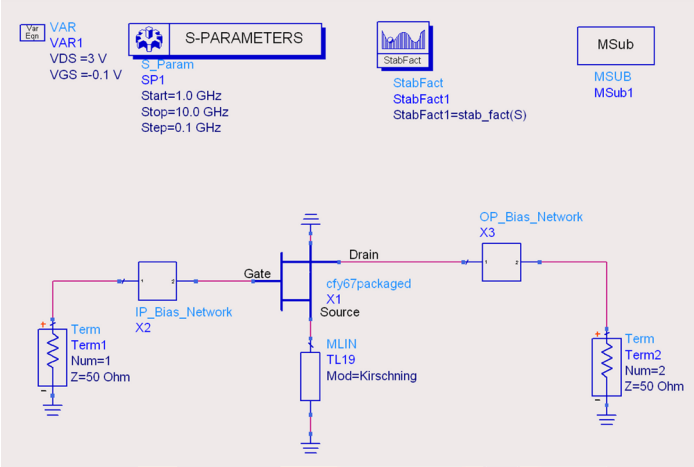


Figure 192.

The results obtained from the circuit above are shown below. Note that the circuit is unstable from ~ 2.1 GHz to 7 GHz and it needs to be stabilized before we can match input and output impedances.

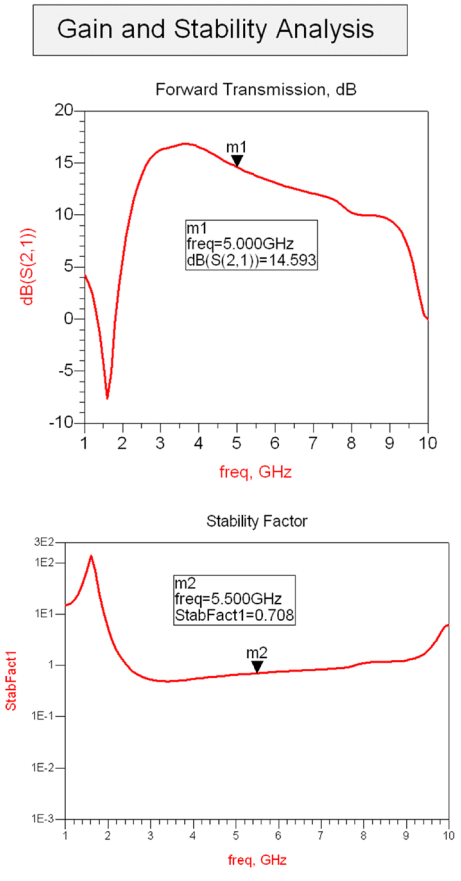


Figure 193.

There are various stability configurations that could be used to stabilize the circuit, the most popular being the use of resistive loading of the circuit depending upon the region of stability and type of amplifier. The illustration below shows one of the techniques to stabilize the circuit.

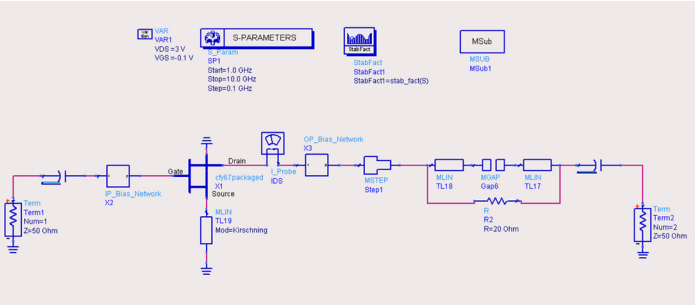


Figure 194.

A stabilized Circuit with Resistive loading at the output side is shown (Please note the modeling of the Resistor layout footprint, which is connected in parallel to the resistor; this will allow us to take care of mismatch or distortion introduced because of the discrete component's footprint.)

One output resistor was used at the output side of the amplifier and then the value of the resistor was tuned to achieve the proper stability. The illustration below shows the results after stabilization.

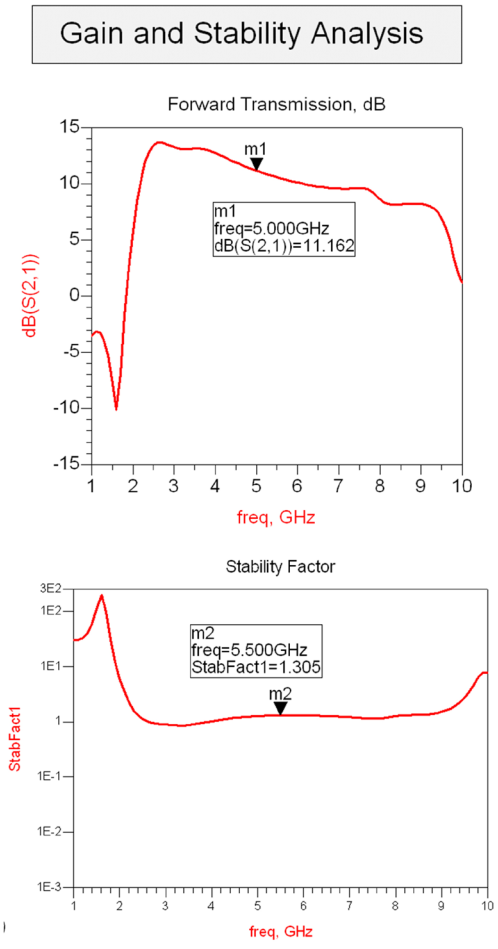


Figure 195.

Input and Output Matching Network Design

After the circuit is stabilized in the broadband range, we can start the design of the input and output matching networks so that we achieve the desired specifications of the amplifier. The illustration below shows the amplifier after adding bias networks, the stability components and the input and output coupling capacitors. Designers must note the proper layout footprint modeling for lumped components in the schematic, as shown in Fig. 196 below so as to take care of the discontinuities that the signal will undergo in a practical circuit. This should accompany each lumped component. This is quite important when designing amplifiers in the microwave range.

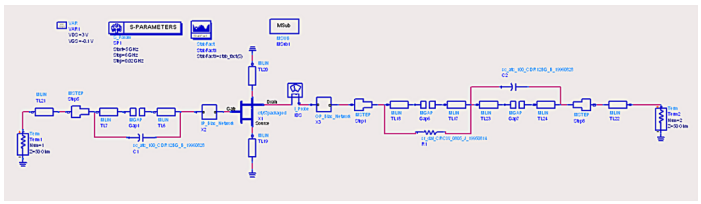


Figure 196.

The choice of matching network topology mainly depends on the bandwidth of the amplifier. Single stub and double stub matching networks can be used. The illustration below shows input and output impedances on the smith chart, which need to be matched with the 50-ohm impedance.

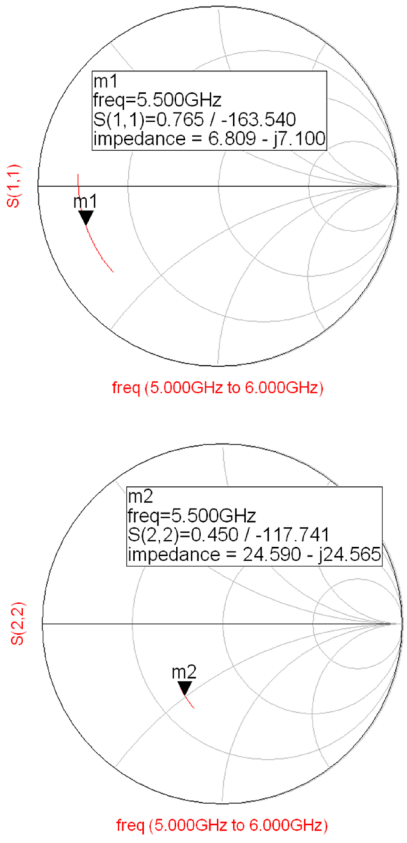


Figure 197.

For the present amplifier design, a double stub approach was used to design the input and output matching networks to achieve the best possible input and output return losses. Refer to the illustrations below for the input and output matching networks that were designed using Matching networks synthesis utility available in the ADS software.

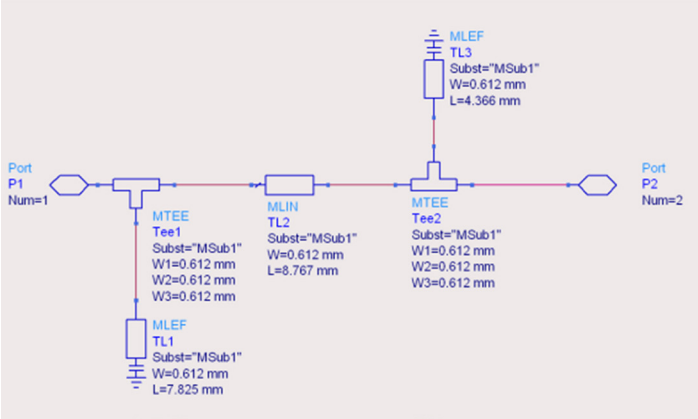
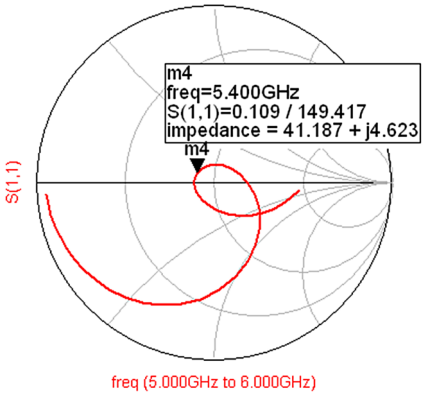


Figure 198.



The following illustrations show the results after connecting input and output matching networks to the amplifier circuit.

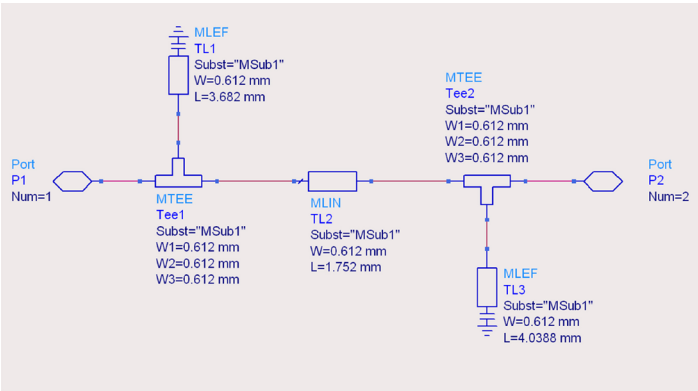


Figure 199.

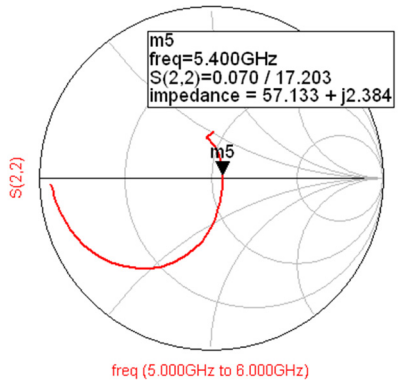


Figure 200.

Overall Amplifier Performance Optimization

The only thing remaining now in the amplifier design is to connect all the sub-networks together, to see the overall amplifier performance and to optimize the overall circuit if needed. The illustration below shows the complete amplifier:

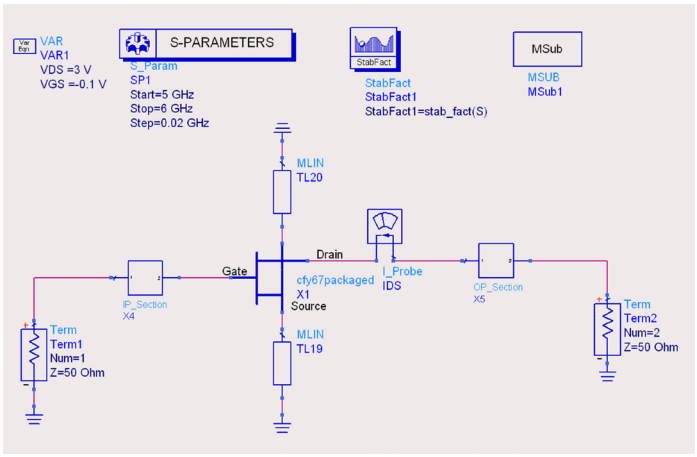


Figure 201.

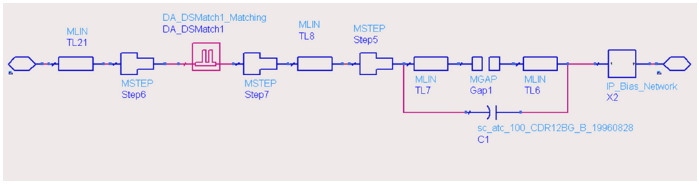


Figure 202.

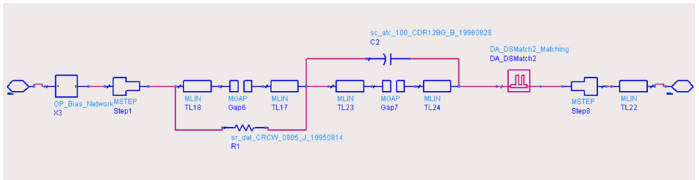


Figure 203.

The following illustration shows the complete layout of the designed amplifier

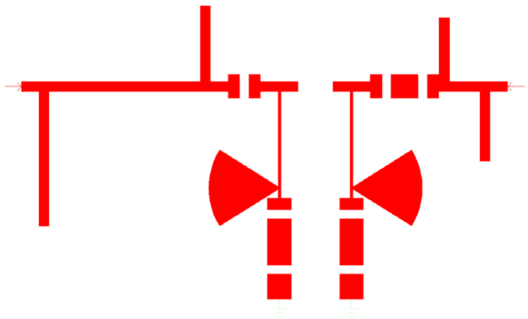


Figure 204.

The following illustration shows the amplifier results. These were obtained after minimal manual tuning of the matching stub lengths to achieve the desired results after each of the blocks together.

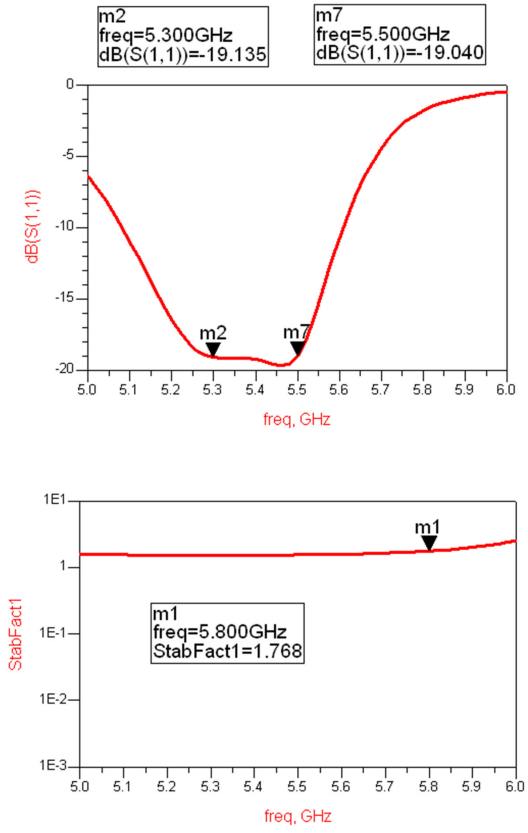


Figure 205.

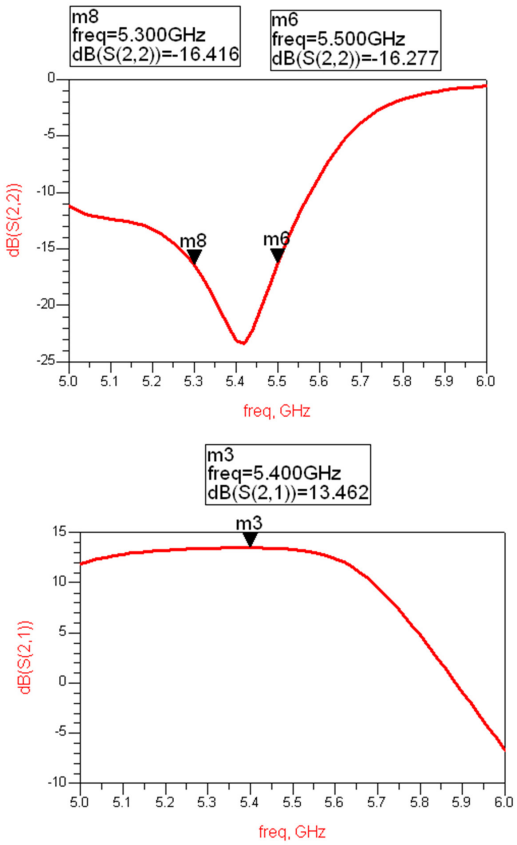


Figure 206.

Conclusion

It can be seen from the procedure above that the amplifier design can be easily done if a well-defined procedure is followed, and that designers can save time spent in fine tuning the amplifier performance optimization.

Statistical Simulations (Monte Carlo and Yield Analysis)

Note: the article below, originally published in the High Frequency Electronics, January 2007 issue with the title “Statistical Analysis of MW circuits predict Real world performance” has been reproduced with permission.

ADS Licenses Used: Linear Simulation, Statistical Design Package

Introduction

To obtain good and predictable circuit performance with all the tolerance variations involved could be very challenging. These tolerances could be due to a specific process used or because of discrete components used in circuit design and for robust circuit and system design these variations need to be accounted for and examined during the circuit or system simulation stages to gain confidence in the design fidelity. This type of simulation is commonly referred to as Statistical analysis. This paper outlines the intricacies of Statistical analysis and makes designers aware of various types of statistical analyses that can be performed to

gain additional confidence during the design process. To illustrate the various statistical simulations, a MIC based C-band amplifier design [1] is used.

Process Variations and Discrete component tolerance

There are multiple sources of variations in the real microwave world that can be associated with Dielectrics, the Etching Process and Discrete components etc.

1. **Dielectrics**: dielectrics can have variations in their height, loss tangent and dielectric constant (Er) and this data can be obtained directly from the manufacturer's datasheet.
2. **Etching**: the etching tolerance in the printed circuit process is dependent upon the etching technique used and this tolerance mainly affects the width of the transmission lines.
    a. Chemical etching process can have tolerance level of +/- Metal Conductor Thickness (max.).
    b. Reactive ion etching can produce the excellent tolerance of +/-1um.
    c. Metal deposition techniques could also produce tolerance of +/- 1-2um
3. **Discrete components**: discrete components like Inductors, Capacitors, and Resistors etc. have their inherent tolerances, which can affect circuit performance. Different tolerances for discrete components are summarized in Table 1.

All of the above mentioned tolerances should be included in the circuit design process as far as possible so that the circuit could be analyzed and optimized over these variations. In the present text, a typical MIC Amplifier circuit is used for statistical simulations and the variations considered are the etching tolerances and discrete component's tolerances to keep the paper simple. The designer can then take this concept and apply this technique to each variation (e.g. dielectric parameter tolerances etc.) in their respective processes.

The substrate which is used for Amplifier design in the present text has following specifications:

- **Dielectric Height**: 25 mils
- **Dielectric Constant**: 9.9
- **Loss Tangent**: 7x10-4
- **Conductor Thickness**: 8 µm
- **Conductivity**: 4.1E+7 (Gold Conductor)

Typical discrete component tolerances are provided in the table below:

Component Class	Tolerance
B	±0.1 (absolute)
C	±0.25 (absolute)
D	±0.5 (absolute)
F	1%
G	2%
J	5%
K	10%
M	20%

Statistical Design

To perform a simulation that can account for real world tolerance variations, the designer needs to understand statistical analysis as discussed below.

Statistical analysis is the process of:

- Accounting for the random (statistical) variations in the parameters of a design.
- Measuring the effects of these variations.
- Modifying the design to minimize these effects.

Yield analysis is the process of varying a set of parameter values, using specified probability distributions, to determine how many possible combinations result in satisfying predetermined performance specifications.

Yield is the unit of measure for statistical design. It is defined as the ratio of the number of designs that pass the performance specifications to the total number of designs that are produced. It may also be thought of as the probability that a given design sample will pass the specifications.

Because the total number of designs produced may be large or unknown, yield is usually measured over a finite number of design samples or *trials* in the process known as *yield estimation*. As the number of trials becomes large, the yield estimate approaches the true design yield. Parameter values that have statistical variations are referred to as *yield variables*.

Three statistical design options that can be used in ADS to analyze circuits are:

Monte Carlo Analysis

Monte Carlo yield analysis methods have traditionally been widely used and accepted as a means to estimate yield. The method simply consists of performing a series of trials. Each trial results from randomly generating yield variable values according to statistical-distribution specifications, performing a simulation and evaluating the result against stated performance specifications.

The power of the Monte Carlo method is that the accuracy of the estimate rendered is independent of the number of statistical variables and requires no simplifying assumptions about the probability distribution of either component parameter values or performance responses.

The weakness of this method is that a full network simulation is required for each trial and that many trials are required to obtain high confidence and an accurate estimate of yield.

Monte Carlo Trials and Confidence Levels

The following text discusses how to calculate the number of trials necessary for a given confidence and estimate error. Confidence level is the area under a normal (Gaussian) curve over a given number of standard deviations. Common values for confidence level are shown in the following table.

Standard Deviations	Confidence Level
1	68.30%
2	95.40%
3	99.70%

Error is the absolute difference between the actual yield, Y, and the yield estimate, $\tilde{Y}$, given by:

$$E = |Y - \tilde{Y}|$$

Where, E is the percent error. The low value limit of $\tilde{Y}$ is given by:

$$\tilde{Y} = Y - E$$

The sample or trial size, N, is then calculated from:

$$N = \left(\frac{C\sigma}{E}\right)^2 * Y(1 - Y) \quad \text{---------- (a)}$$

where, $C\sigma$ is the confidence expressed as a number of standard deviations.

Example
For a 95.4% confidence level (i.e. Standard Deviation=2), an Error = +/-2% and a yield of 80%

$$N = \left(\frac{2}{0.02}\right)^2 * 0.8(1 - 0.8)$$

N=1600 trials

Yield analysis:
This process involves simulating the design over a given number of trials in which the yield variables have values that vary randomly about their nominal values with specified probability distribution functions. The number of passing and failing trials are recorded and these numbers are used to compute an estimate of the yield. Basically, Yield means the percentage of circuits that meet the desired specifications set as Goal by the designer.

Yield analysis is based on the Monte Carlo method. A series of trials is run in which random values are assigned to all of a design's statistical variables, a simulation is performed, and the yield specifications are checked against the simulated measurement values. The number of passing and failing simulations is accumulated over the set of trials and used to compute the yield estimate.

Confidence Tables:
The confidence tables that can be followed to determine the number of trials suitable for a yield analysis for different confidence levels and a yield of 90% are given below. For more tables, designers can refer to the software documentation [2].

Confidence=68.3% ***Actual Yield=90%***

Error ± %	Estimated % Yield		Number of Trials
	Low	High	
1	89	91	900
2	88	92	225
3	87	93	100
4	86	94	56
5	85	95	36
6	84	96	25
7	83	97	18
8	82	98	14
9	81	99	11
10	80	100	9

Confidence=95% ***Actual Yield=90%***

Error ± %	Estimated % Yield		Number of Trials
	Low	High	
1	89	91	3457
2	88	92	864
3	87	93	384
4	86	94	216
5	85	95	138
6	84	96	96
7	83	97	70
8	82	98	54
9	81	99	42
10	80	100	34

Confidence=99% ***Actual Yield=90%***

Error ± %	Estimated % Yield		Number of Trials
	Low	High	
1	89	91	5967
2	88	92	1491
3	87	93	663
4	86	94	372
5	85	95	238
6	84	96	165
7	83	97	121
8	82	98	93
9	81	99	73
10	80	100	59

Yield optimization:
Yield optimization adjusts nominal values of selected element parameters to maximize yield. Also referred to as design centering, yield optimization is the process in which the nominal values of yield variables are adjusted to maximize the yield estimate.

To have control over the confidence level and hence the accuracy of the yield estimate, it is recommended that designer perform a yield analysis after the yield optimization is completed, using the nominal parameter values obtained from the yield optimization. An appropriate number of trials can be chosen based upon the formula mentioned in the table above.

Performing Statistical analysis without a good simulation tool is not practical due to the large number of trials involved. The simulation tool should have the capability to perform Yield Analysis, Monte Carlo Analysis and Yield Optimization to make sure that the designed circuit has the capability to sustain real world variations.

Example - Statistical Analysis of a C-Band MIC Amplifier
The following illustration shows a complete schematic design for C-band MIC amplifier

Amplifier Specifications:

- Frequency Band: 5.3 GHz – 5.5 GHz
- Gain: 13 dB (min)
- Input Return Loss: < -15 dB
- Output Return Loss: < -15 dB

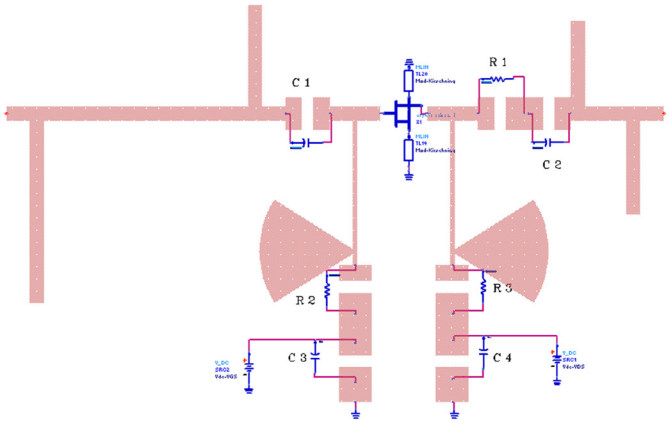
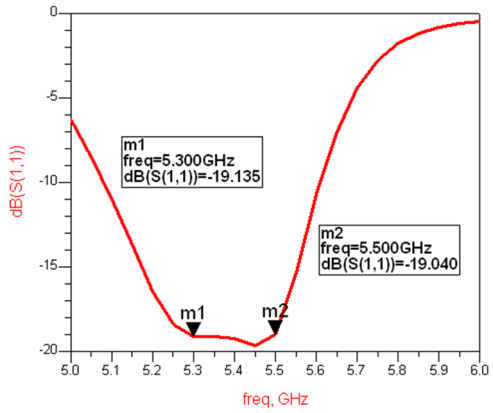
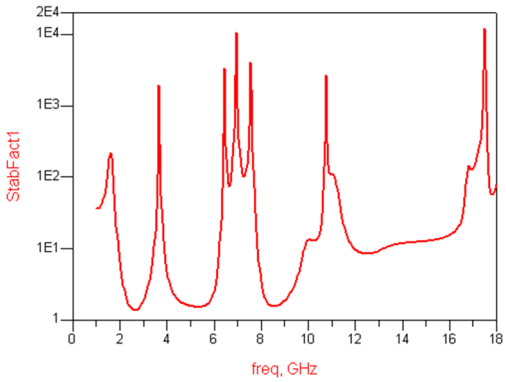


Figure 207.

Below illustration shows optimized circuit performance:





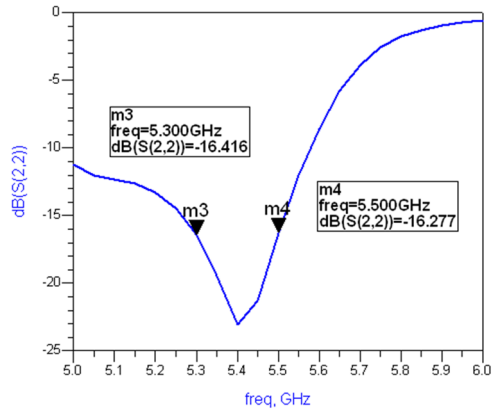


Figure 208.

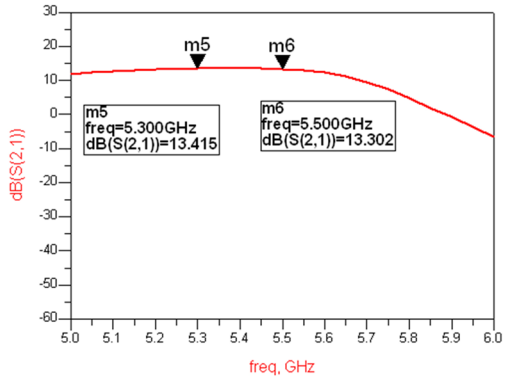


Figure 209.

The amplifier is designed on a 25-mil Alumina substrate as mentioned in (2) above and, considering the chemical etching process, the maximum etching tolerance would be @+/-8um and uses several discrete components as given in table below:

Component	Value	Tolerance	Purpose
R1	24 Ω	5%	Stability
R2	300 Ω	5%	Stability (input bias line)
R3	10 Ω	5%	Stability (output bias line)
C1	2 pF	±0.1 pF	Coupling capacitor (input)
C2	2 pF	±0.1 pF	Coupling capacitor (output)
C3	560 pF	10%	Bypass capacitor (input)
C4	560 pF	10%	Bypass capacitor (output)

Three steps are needed in order to perform statistical analysis:

a. Define the tolerance on the components/transmission lines
b. Setup the performance yardstick to be met
c. Defining the number of trials and selecting of the Statistical analysis method (Monte Carlo or Yield Analysis)

All the transmission line widths were given the statistical variation of +/-8um using a Gaussian distribution function and the discrete components were provided with the mentioned tolerance as mentioned in the table above.

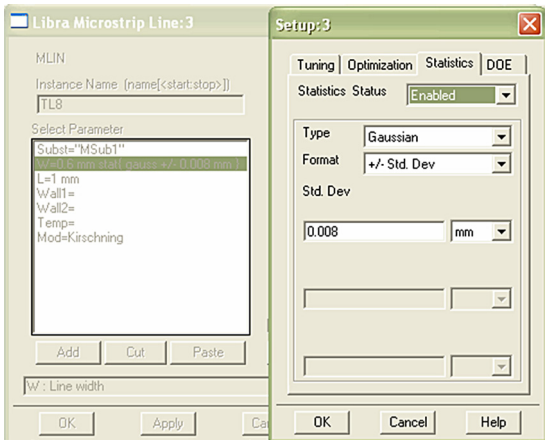


Figure 210.

The performance yardstick to be met was set as stated in the Amplifier Specification and shown in the following illustration.

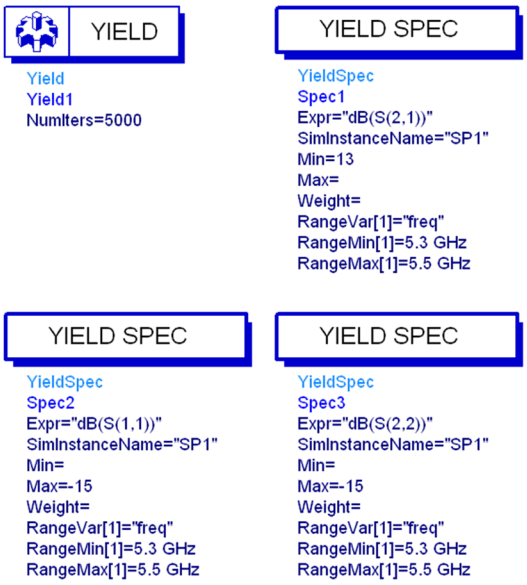


Figure 211.

The number of trials was selected as 5000 and the yield analysis method was selected to view the pass percentage after the statistical analysis. The initial results obtained are displayed below and show the yield percentage to be @81% . This is fairly good for a first iteration. The table below also shows the number of circuits that passed the required specification and the number of circuits that failed.

Yield	NumFail	NumPass
80.940	953.000	4047.000

For actual production, the yield should be at least >90-95%. After running an initial yield analysis, the designer has the choice of performing a Yield Optimization or Sensitivity Analysis to improve the yield (not discussed in this article).

To obtain the reason for lower yield, another yield analysis was performed with only 250 iterations and data for each iteration was saved to have a closer look at the specifications that were not complying with the yield specifications and are shown in the figure above.

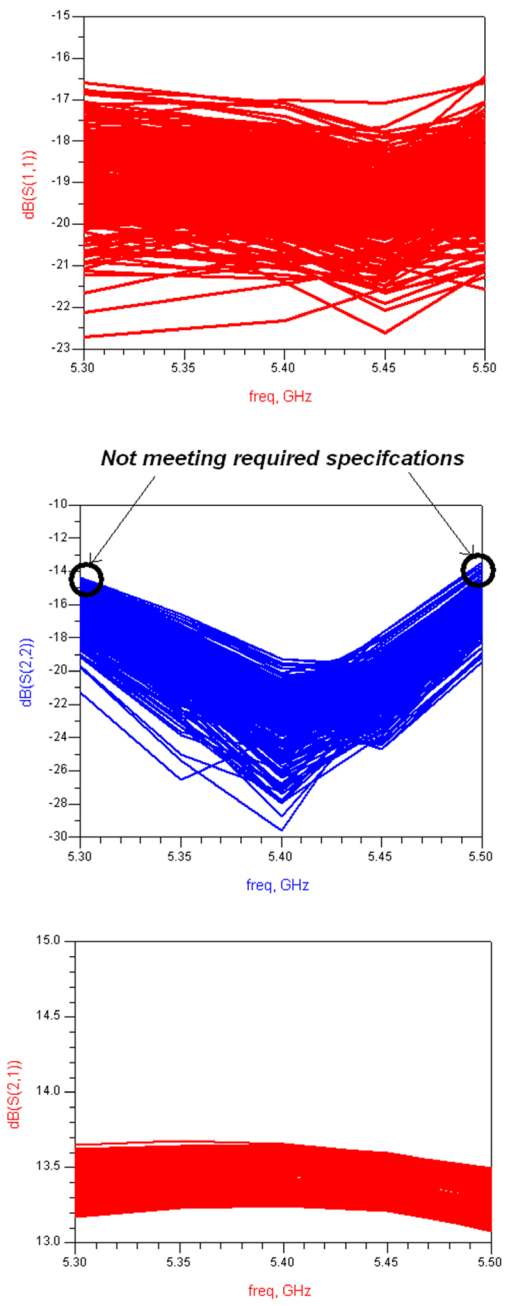


Figure 212.

Yield	NumFail	NumPass
82.000	45.000	205.000

It can be seen from the illustrations above that Input Return Loss and Gain specifications have no contribution in lowering yield. The main culprit for lower yield is the Output Return Loss, which is **slightly** below the desired specification on the lower and upper band edges. Designers can perform Yield Optimization to center the design to account for these statistical variations.

Looking at the results above it can be seen that although the yield percentage figure is not looking good as a percentage number, the output return loss is just a fraction lower than the required specification. Another round of yield analysis was performed with the target specification for the output return loss (S22) changed to -14 dB. An excellent yield of 98.5% was obtained, which is shown in the table below.

Yield	NumFail	NumPass
98.500	75.000	4925000

Conclusion

It can be seen that performing yield analysis is essential before going to production. Using sophisticated simulation tools, designers have the flexibility to perform complex statistical simulation with great ease and can increase the reliability of the designed circuits.

Additional Information on Yield Analysis:
Additional material and various Statistical simulation examples can be found at the Keysight EEsof EDA Knowledge Center. Designers can register at:

http://www.keysight.com/find/eesof-knowledgecenter

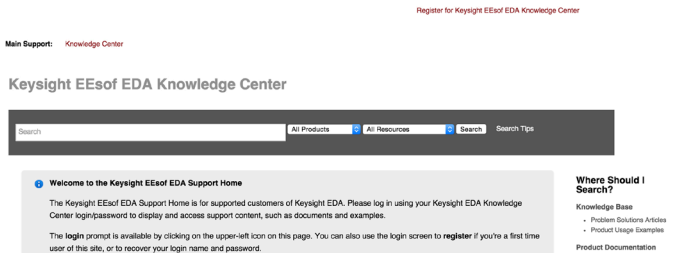


Figure 213.

Registered users can find additional technical notes and examples on Yield Analysis at:

https://edasupportweb.soco.keysight.com/

MESFET Frequency Multiplier Design

Article originally published in Microwave Journal, June2003 issue, reproduced with permission

ADS Licenses Used: Linear Simulation and Harmonic Balance

Abstract

The design of nonlinear circuits is usually viewed as a challenge; the foremost reason being the difficulty in determining accurate models to describe device behavior over a wide range of conditions, including varying frequency and power levels.

A practical and straight-forward approach to nonlinear microwave circuit development is to use any of the non-linear circuit simulators as a substitute to constructing many prototypes and thus saving time and effort. This paper intends to collect the theory of MESFET Frequency multipliers and to show how to design a MESFET Multiplier using simple simulation procedures without going into much of the theoretical aspects of MESFET Multiplier design. Formulae to design multipliers are provided here for those who are interested in the theory. This paper will provide insights to MESFET multiplier design & simulation to help the engineers working in this arena of Non-linear Microwave.

Introduction

The illustration below shows a generalized circuit schematic of a MESFET frequency multiplier. The basic principal of operation of a MESFET multiplier is that the device is operated for a particular conduction angle based on the harmonic frequency to be generated. Table 1 shows the Fourier components as function of conduction angle up to the 5th harmonic. It can be seen that the generalized circuit shown here appears to be identical to the power amplifier; the only difference is that the output resonator is tuned to the nth harmonic of the fundamental, not the fundamental frequency.

FET Multiplier Over SRD Multipliers

Unlike diodes, MESFET's currents cannot be described by a single equation and thus require a more complex treatment to describe their nonlinear operation. Comparison of MESFET and Schottky diode multipliers is not simple and requires engineering judgment for the specific application. For instance, frequency doublers built with Schottky-barrier diodes, are lossy (in general >10dB), require no tuning elements, and can operate over an octave bandwidth, a performance that cannot be attainable with MESFETs. On the other hand, if bandwidth is less than 50%, MESFET multipliers have great advantage over SRD multipliers as FET multipliers can achieve a conversion gain that is greater than unity (generally kept as unity) depending upon the bandwidth while maintaining good dc-RF efficiency.

However, intuitively we can conclude that transistors offer several other advantages compared to diodes viz., isolation from input to output so that usually it suffices to match the input at the fundamental frequency, and the use of only a bandpass filter at the output. They also require much less drive power for generating significant output power levels. An additional advantage of MESFETs is that they are a natural part of MMIC's where power efficient frequency multipliers can be designed to fit a specific need, which saves weight, size and power consumption. These factors are always of great importance in Deep Space Missions or even in terrestrial satellites.

Non-Linearities Involved in MESFETs

There are three non-linearities that can be utilized to generate harmonic frequencies.

Gate-Source Capacitance (C_{gs})

The first is the use of the FET gate-source capacitance (C_{gs}). This non-linearity has been analyzed as a lossy varactor that resulted in harmonic frequency signal levels of -18 to -11 dB below the expected fundamental frequency output power level.

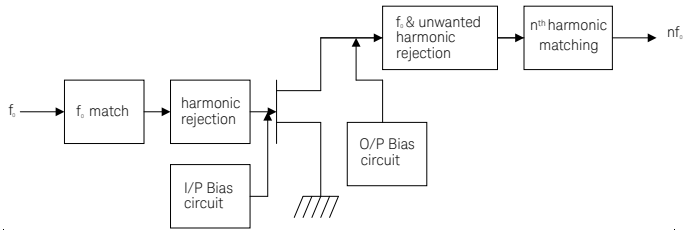


Figure 214.

Fourier frequency components						
n	$\emptyset_t$	I_1/I_p	I_2/I_p	I_3/I_p	I_4/I_p	I_5/I_p
1	360°	-6.0 dB	–––––	–––––	–––––	–––––
2	120°	-8.4 dB	-12.0 dB	-17.0 dB	-32.0 dB	-24.0 dB
3	76°	-12.0 dB	-13.2 dB	-15.4 dB	-18.4 dB	-20.0 dB
4	65°	-13.4 dB	-15.4 dB	-15.9 dB	-18.0 dB	-18.4 dB
5	48°	-14.7 dB	-14.9 dB	-16.4 dB	-18.2 dB	–––––
Pinch-off	180°	-6.0 dB	-13.2 dB	–––––	-27.0 dB	-17.9 dB
Square-wave	360°	-3.9 dB	–––––	-13.5 dB	–––––	–––––

Drain-Source Characteristics

The second non-linearity arises from clipping of the Ids wave-form. This effect can be induced by biasing the device at **0 V or at pinch-off** and causing a half-wave rectified sinusoidal output voltage that has a theoretical second harmonic level of 7.4 dB below the fundamental frequency output signal.

V_{gs}-I_{ds} transfer characteristics

The third non-linearity is due to the non-linear V_{gs}-I_{ds} transfer characteristic. FET devices generally exhibit good linearity and as a result, this feature does not contribute significantly to multiplier performance.

Simulations using a unilateral FET model have shown that the non-linearity with the greatest contribution to harmonic generation is the clipping of the I_{ds} waveform with less significant contributions from C_{gs} and transfer non-linearities.

In order to optimize the harmonic generation of the frequency multiplier, attention must be paid to the terminations [3-6] that are presented at the device output to the fundamental and n^{th} harmonic frequency signals. Biasing the gate at 0 V (or pinch-off) to create a half-wave rectified output will provide better conversion efficiency if the fundamental frequency signal is terminated in an open circuit and the n^{th} harmonic frequency is extracted by a matched load. This allows a maximum voltage swing of the rectified sinusoidal waveform, which is rich in n^{th} harmonic signal content.

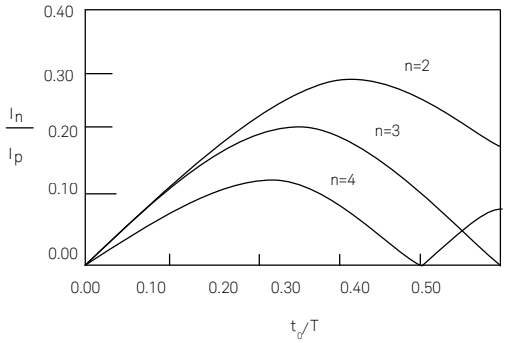


Figure 215. Harmonic drain-current components as a function of to/T when the drain-current waveform is a half-sinusoidal pulse train.

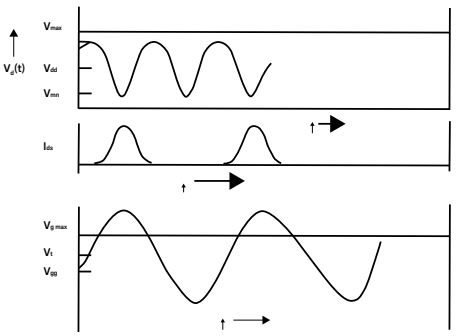


Figure 216. Voltage and Current waveform of an ideal MESFET Frequency Multiplier.

Selection of a Non-Linear Model for MESFET

Selection of the proper non-linear model for the device to be used for Simulation purposes plays a very important role in designing a non-linear circuit accurately. Non-linear MESFET device models such as Statz, Curtice Cubic, TOM etc. Distinctions of these three models are given below and the user can select an appropriate model to aid in selecting an appropriate device. There may be slight differences in the way a model is implemented in commercial simulators. Although the same model exists in multiple simulators, each simulator may use slightly different variable names. For example, most GaAs FET models contain a zero bias gate-source junction capacitance. In PSPICE and MDS this capacitance is defined as the variable CGS; in LIBRA and COMPACT it is defined as CGSO. These differences require the user to translate model parameters to conform to the syntax of their specific simulator to be used for circuit simulation purposes.

Statz Model

The Statz model is more accurate when the Ids for a device behaves quadratically (square-law approximation) for the small values of (V_{gg} - V_p) and linearly for large value of (V_{gg} - V_p).

Curtice Model

The Curtice model is useful when extracting a model at a single bias point.

Triquint's Own Model (TOM)

TOM is more accurate when the square-law approximation does not predict device performance well and when the device drain conductance varies with gate-source bias.

Note:
More details on non-linear models can be obtained from ADS software documentation.

Design of a FET Frequency Multiplier

- The design of a frequency multiplier can be initiated by selecting the appropriate Gate voltage to control the conduction angle of the FET keeping in mind the prominent harmonic to be generated. Also, the appropriate Drain voltage needs to be selected. The peak reverse voltage across the gate has to be taken into account if the MESFET is being biased much below the pinch-off voltage (i.e. if $V_{gg} << V_t$). The typical reverse voltage across the gate can be approximated by the expression $2V_{gg} – V_{g,max,}$ a relatively high reverse voltage.
- The input bias network typically includes a high impedance line of λ/4 length at f_o (fundamental frequency) so that no fundamental power goes into the DC bias, which is connected via a bypass capacitor to ground in parallel. The high impedance line of λ/4 length at f_o becomes λ/2 length at $2f_o$ (second harmonic) frequency so it acts as a short circuit at the second harmonic frequency.

The Gate's short circuit at the second harmonic frequency is less critical; a shorted stub λ/4 long at fundamental frequency is adequate to provide the termination. Similarly, a high impedance line of λ/4 length at the output center frequency (nf_o) was used for Drain biasing purposes, which was connected via a bypass capacitor to ground in parallel.

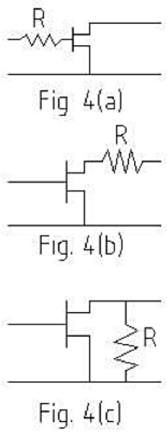


Figure 217. Stabilization Techniques

The most important thing, which needs to be addressed carefully, is the stability of the circuit. If the circuit is not stable over the full frequency band then it needs to be stabilized; any of the stabilization techniques shown in the illustration above can be used to serve the purpose. Although any of the topology can be used but, care must be taken in employing the best possible configuration according to the stabilizing requirement of the circuit and also keeping the RF power dissipation to the minimal extent due to stabilization components.

The stability of the circuit is of utmost importance and the stability factor (K) of the circuit has to be greater than '1' no matter if some of the conversion gain of the multiplier needs to be sacrificed.

- Rejection of the other unwanted harmonics present in the output can be accomplished by proper open or short-circuited stub arrangement. These stubs could be open or short-circuited stubs based on the convenience and the size of the circuit. The open-circuited stubs of λ/4 length on various harmonic frequencies can be connected in shunt to the drain so that drain sees a short circuit load at unwanted harmonics. The nominal widths of these shunted stubs could be 50-ohms or other depending on circuit requirement.

If the multiplier needs to be realized for a moderate bandwidth, then a Bandpass filter could be connected at the output to get the best possible flatness over the entire output band. The open or short-circuited stubs that are used for rejection of unwanted harmonics in the output tend to limit the bandwidth due to their dispersive effect. The choice of the topology of the Bandpass filter depends on the individual's judgment and the system lineup requirements. For example, if the output frequency is high (near Ku-band) then a half wave filter which consists of cascaded alternate lines of high and low impedances of length λ/2 at desired harmonic frequency would be a good choice. This filter will provide moderate to high bandwidth without consuming too much of space in the circuit and if the output frequency lies in the C-band then a Hairpin bandpass filter topology will be a good choice to get the required rejection of the harmonics present in the output, also the space occupied will be less than that in the case of a Coupled line bandpass filter topology. If the size requirement of the circuit is not critical, then a Coupled line filter can be used in the output.

What remains is to match the input and output sections of the circuit to the 50-ohm source and load terminations.

For this purpose, the use of Large Signal S–parameter simulation is available in all the RF/Microwave Non-linear simulators. These are power dependent parameters and the required power source needs to be connected at the input of the device.

The circuit can be re-optimized for better performance in Conversion gain, input / output return loss etc. using the non-linear simulator.

Simulation of MESFET Frequency Multiplier

The simulated design presented here is for the MESFET Frequency Tripler using the non-linear ATF21170 MESFET model available in the Keysight ADS RF transistor library at the input frequency of 1500 MHz with a input bandwidth of ± 50 MHz. The gate and drain bias was fixed based on the maximum output power at the required 3rd harmonic after simulating the MESFET for an input power of +4dBm using the Harmonic Balance analysis of ADS. The peak reverse voltage across the gate was also taken into account so that it doesn't cross the maximum specified limit of the MESFET used for the design.

The input and output bias network was then designed by using a high impedance quarter wavelength (λ/4) line at input and output center frequencies respectively.

First, the stability of the circuit was established after deciding the Gate and Drain voltages and designing the input and output bias network. The linear S-parameter simulation of ADS was used for this purpose. The circuit was not stable over the full frequency band so a resistor was connected in series with the gate (Rs1) and one series resistor (Rs2) and capacitor (Cs1) combination was connected in shunt with the gate. The values of the Resistors were tuned till the stability factor of greater than '1' was achieved. Care was taken to keep the value of the resistor in series with the Gate to be as minimum as possible so that it doesn't consume much input power and also the value of the shunt resistor was kept as large as possible.

A 3-section coupled line Bandpass filter at the center frequency of 4500 MHz (3rd harmonic) was connected at the output to provide nominal rejection of the unwanted harmonics at the output. The Coupled Line topology was selected for the Bandpass filter because of available space for the circuit, any other topology will also serve the purpose if the size of the circuit is of major concern.

The large signal S-parameters of the circuit were simulated using ADS and the input and output matching network was designed so as to match the Gate and Drain impedance with 50-ohm source and load terminations. In the present case, a single open circuited stub on each side (input & output) was sufficient to match the circuit over the entire bandwidth.

The circuit was re-optimized for better conversion gain, input and output return loss and passband flatness in the output after completing design of all the sub-networks. The complete layout for the frequency tripler circuit is shown in the illustration below.

The circuit was designed and fabricated on 25-mil Alumina substrate with a dielectric constant (Er) of 9.90.

Design Formulas for the Multiplier

The drain current of a FET is given by:

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gg}}{V_p}\right)^2 \quad \text{---------- (1)}$$

The conduction angle of the FET can be calculated using the following expression

$$\theta_t = 2\cos^{-1}\left(\frac{2V_t - V_{g,max} - V_{g,min}}{V_{g,max} - V_{g,min}}\right) \quad \text{---------- (2)}$$

The bias voltage that achieves this value of θ_t is

$$V_{gg} = \left(\frac{V_{g,min} + V_{g,max}}{2}\right) \quad \text{----------(3)}$$

The current in the load resistor, R_L, is I_n. For the voltage V_L across the load to vary between V_{max} and V_{min}

$$\left|V_L(t)\right| = I_n R_L = \left(\frac{V_{max} - V_{min}}{2}\right) \quad \text{----------(4)}$$

The Optimum load resistance is

$$R_L = \left(\frac{V_{max} - V_{min}}{2I_n}\right) \quad \text{---------- (5)}$$

R_L in a multiplier is usually much greater.

The output power at the n^{th} harmonic, $P_{L,n}$ is

$$P_{L,n} = \frac{1}{2} I_n^2 R_L = \frac{1}{2} I_n \frac{V_{max} - V_{min}}{2} \quad \text{---------- (6)}$$

As with a power amplifier, the dc drain bias voltage is halfway between V_{max} and V_{min} that is,

$$V_{dd} = \frac{V_{max} + V_{min}}{2} \quad \text{---------- (7)}$$

The dc power is given by the expression

$$P_{dc} = V_{dd} I_{dc} = \frac{1}{2} V_{dd} I_o \quad \text{----------(8)}$$

So, the dc-RF efficiency can be written as

$$\eta_{dc} = \frac{P_{L,n}}{P_{dc}} \quad \text{---------- (9)}$$

The input power can be approximated by the expression

$$P_{av} = P_{in} = \frac{1}{2}(V_{g,max} - V_{gg})^2 \omega_p^2 C_{gs}^2 (R_s + R_i + R) \text{---(10)}$$

$$\text{Conversion Gain} = \frac{P_{L,n}}{P_{av}} \quad \text{---------- (11)}$$

The power added efficiency of a FET multiplier is

$$\eta_a = \frac{P_{L,n} - P_{in}}{P_{dc}} \quad \text{---------- (12)}$$

or,

$$\eta_a = \eta_{dc}\left(1 - \frac{1}{G_p}\right) \quad \text{---------- (12a)}$$

The maximum drain-gate voltage is approximately V_{max} - $V_{g,min,}$ so we have the limitation V_{max} - $V_{g,min}$ < $V_{a,}$ where V_a is the drain-gate avalanche voltage.

Where, G_p is the power gain ($P_{L,n}/P_{in}$) of the multiplier.

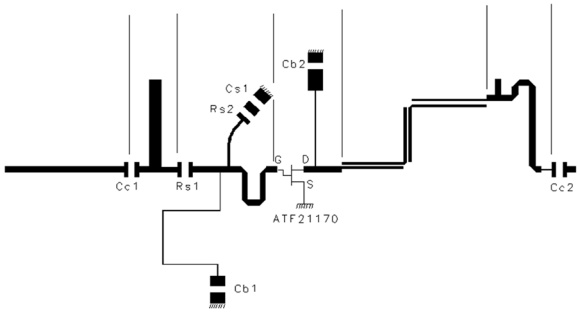


Figure 218. Complete Layout of simulated MESFET Frequency Tripler using ATF21170 under bias condition of Vgg=-0.5 V and Vdd=3.0V and input power of +1 dBm.

Simulated and Measured Results

All the simulated results obtained using Keysight's ADS for the Frequency Tripler are shown in Fig. 219, 220, 221 and 222. Figures 223 & 224 shows the measured results.

Fig. 219 shows the simulated time domain waveform of the Fundamental and 3rd harmonic current at the output of MESFET. The third harmonic current waveform is shown as the thick curve with the amplitude on the left Y-axis. The fundamental current waveform is shown by the thin curve and the amplitude is shown on the right Y-axis.

Fig. 220 shows the simulated time domain waveform of the Fundamental and 3rd harmonic voltage at the output of the MESFET. The third harmonic voltage waveform is shown as the thick curve with the amplitude is on the left Y-axis. The fundamental voltage waveform is shown as the thin curve with the amplitude shown on the right Y-axis.

Fig. 221 shows the simulated Power Spectrum of the ATF21170 Frequency Tripler. The conversion loss of –1.6 dB was achieved in the simulation for the required third harmonic and the Sideband rejection achieved was greater than 20 dB.

Fig. 222 shows the simulated output band flatness of the 3rd harmonic that was achieved to ±0.36 dB in simulation.

Fig. 223 shows the measured Power Spectrum of the Frequency Tripler. The conversion loss of –2 dB was measured (which is –0.4 dB more than the simulated results). The sideband rejection of greater than 20 dB was measured.

Fig. 224 shows the measured output band flatness of the 3rd harmonic. The measured flatness achieved was ±0.30 dB

Simulated Results:

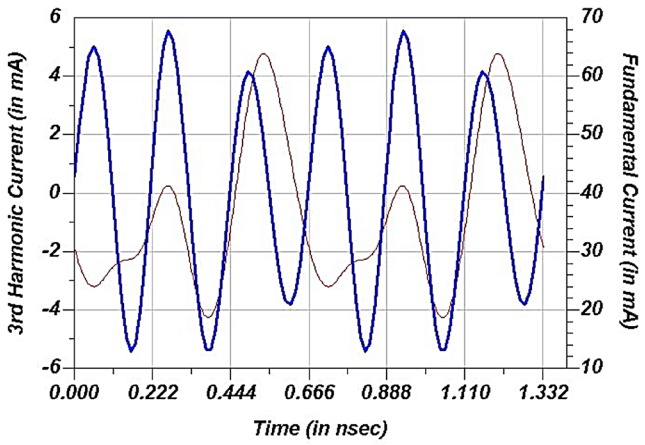


Figure 219. Simulated Time Domain Fundamental & 3rd Harmonic Current waveform

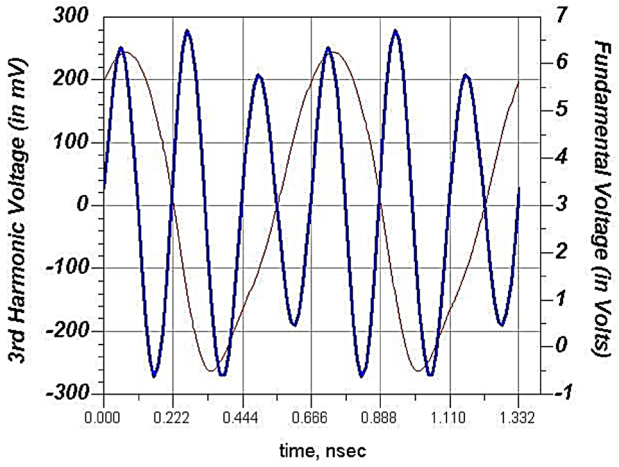


Figure 220. Simulated Time Domain Fundamental & 3rd Harmonic Voltage waveform

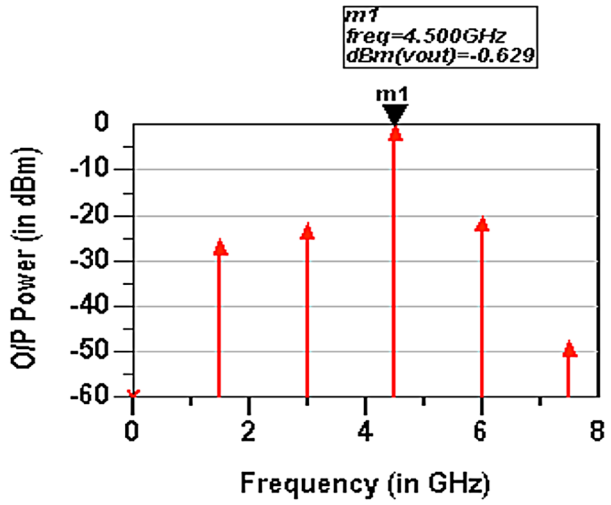


Figure 221. Simulated Output Power Spectrum of Frequency Tripler

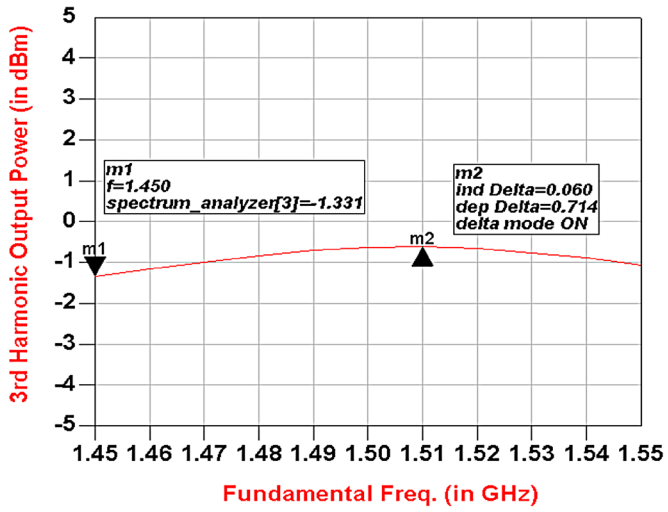


Figure 222. Simulated Output band Flatness of Frequency Tripler

Measured Results:

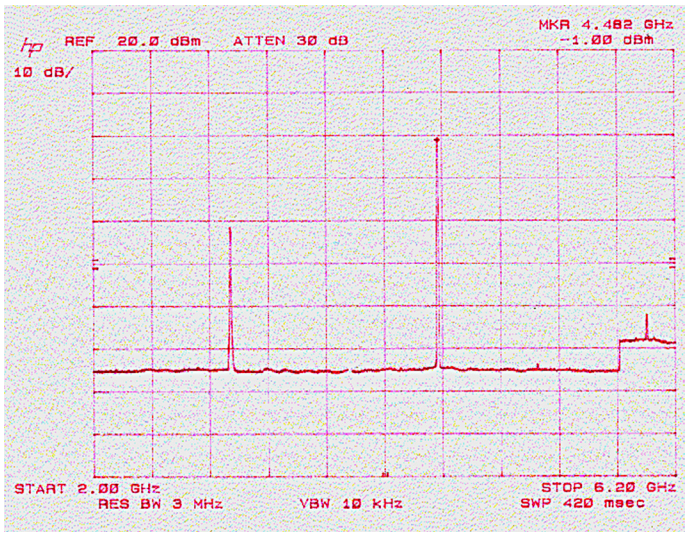


Figure 223. Measured Output Spectrum of Frequency Tripler

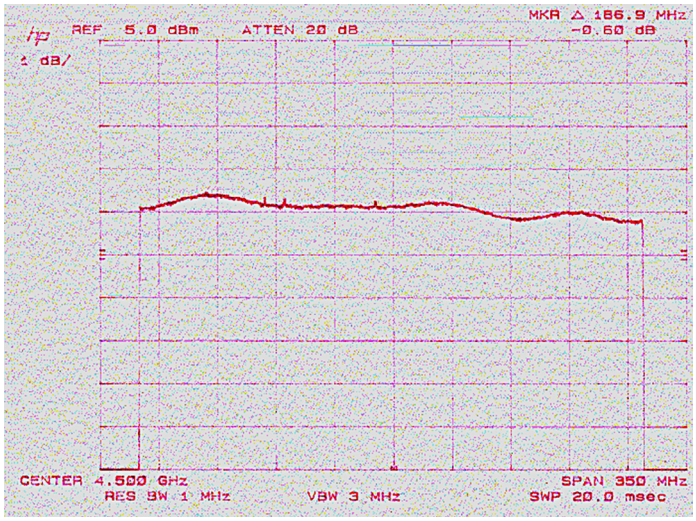


Figure 224. Measured Output band Flatness of Frequency Tripler

List of symbols used

I_{ds} : Drain current

I_p : Peak Drain current

θ_t : Conduction Angle

V_p : Pinch-off voltage

V_{gg} : Gate bias voltage

$V_{g,max}$: Max. gate voltage

$V_{g,min}$: Min. gate voltage

R_L : Load resistance

I_n : Current in nth harmonic

$P_{L,n}$: O/P power at nth harmonic

V_{dd} : Drain bias voltage

P_{dc} : DC power

η_{dc} : dc-RF efficiency

η_a : Power added efficiency

G_p : Conversion gain

P_{in} : Input power

E_r : Dielectric constant

C_{gs} : MESFET Gate-Source Capacitance

V_t : Turn on voltage of MESFET

$P_{L,n}$: nth harmonic output power

P_{dc} : DC Power

t_o/T : Duty cycle

K : Stability Factor

References

[1] Stephen A. Mass, "*Nonlinear Microwave Circuits*", Artech House

[2] Erik Boch, "A High Efficiency 40 GHz Power FET Frequency Doubler", Aug.1989, *Microwave Journal*.

[3] E. Camargo, R. Soares, R.A. Perichon and M. Goloubkoff, "Sources of Nonlinearity in GaAs MESFET Frequency Multipliers", *IEEE MTT-S Digest, 1983, pp. 343-345*.

[4] C. Rauscher, "High-Frequency Doubler operation of GaAs Field-Effect Transistors", *IEEE MTT, Vol. MTT-31, No.6, June 1983, pp. 462-473*.

[5] A. Gopinath and J.B. Rankin, "Single Gate MESFET Frequency Doublers", *IEEE MTT, Vol. MTT-30, No.6, June 1982, pp. 869-875*.

[6] Camargo, Edmar, "Design of FET Frequency Multipliers and Harmonic Oscillators", Artech House

[7] Gonzalez, Guillermo, "*Microwave Transistor Amplifiers Analysis and Design*", Prentice-Hall, Inc.

[8] CEL Application note 'AN1023'

Active Mixer Design

ADS Licenses Used:

1. *Linear Simulation*
2. *Harmonic Balance*
3. *Layout*

Taken from Keysight EEsof EDA Technical Note: Low Power Mixer Design Example Using Advanced Design System

Introduction

This note describes a method for designing a low-power single-transistor active mixer using Keysight Advanced Design System (ADS). It includes details on the design steps, simulation setups and data displays. The workspace file discussed in this lab is available under the ADS example directory */examples/RF_Board/MixerPager_wrk.7zap*. Unarchive the workspace in the working directory by selecting **File > Open > Example > RF_Board > MixerPager_wrk.7zap** and selecting the working directory to unarchive the example workspace.

Circuit Specifications

The mixer is an upper-sideband down converter, with an RF of 900 MHz RF, and a 45 MHz IF. The simplified specifications supplied for this design call for it to provide a 10dB conversion gain, operating from a 1 volt DC supply at 600uA current. This very low power consumption is typical of applications such as pagers and cellular phones, where battery lifetime is critical. Low cost is another driving factor in such applications. Other typical specifications a mixer would have to meet in a "real-world" design, such as linearity, port-to-port isolation, spurious response and noise figure, are not included in this particular example. See */examples/RFIC/Mixers_wrk.7zap* for examples of how to include these simulations in your design.

Device Selection

One of the first steps in the design process is to select the device. The device used for this example is the Motorola MMBR941, a bipolar junction transistor (BJT) packaged in a standard SOT-23 plastic package. While bipolar devices do not generally have as good of mixing properties as field-effect transistors, the low operating voltage precludes using FETs in this case. The chosen device has acceptable performance for this application, and offers several other advantages: it is extremely low cost, and accurate models are readily available. A rule of thumb in high-volume, low-cost applications is to use the least expensive device that will accomplish the job, the MMBR941 is a good choice for this mixer. It is equally true that, no matter how good a device is, if there are no models with which to simulate it, it becomes impossible to use in a design.

The device model, taken from the ADS RF Transistor Library, is a Gummel-Poon model where the parameters were extracted by the manufacturer, Motorola. Initially, the model's DC performance is verified by comparing DC I-V curves. Next, a bias network will be designed to establish the desired operating point. The model's RF behavior will then be checked by comparing the simulated S-parameters with measured S-parameters taken at the same bias conditions. Finally, the model's nonlinear performance is verified by simulating gain compression and comparing to measured results.

Device Model DC Verification (Cell: DC_curves)

DC_curves.dsn (see illustration below) shows one way to set up a swept-parameter DC analysis. The DC voltage supply at the collector is set to a variable, VCE, which is initialized in the VAR block. The VAR block also initializes the variable, IBB, used in the DC current source at the base of the BJT. The actual values used for VCE are determined in the DC simulation controller (DC1). In this example, VCE is swept from 0V to 6V, so that the model can be verified over a relatively wide operating range. The DC controller can only sweep a single variable, so the values for IBB are swept using the ParamSweep component. The range chosen for the base current, IBB, is set to 50uA to 350uA. This IV characteristics simulation setup is available as a default template in ADS and designers can obtain the same under Schematic page by selecting: **Insert > Template > BJT Curve Tracer**, it can be used after setting IBB and VCE values as desired by designers.

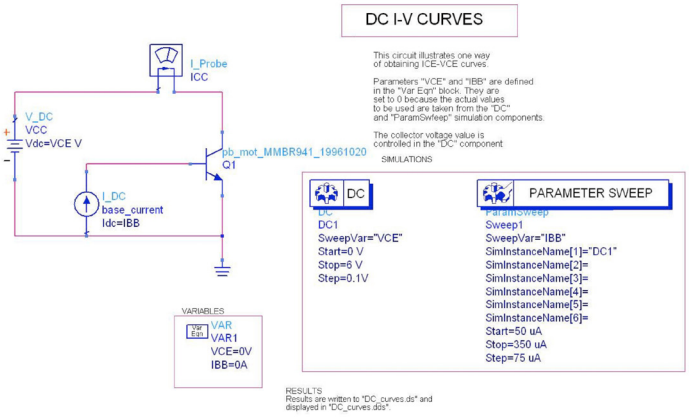


Figure 225. Transistor Swept-Parameter DC Analysis Setup

Results from this simulation are displayed in "DC_curves.dds". The available output variables can be viewed by either placing a new plot or selecting the existing plot for edit, which open the Insert Plot dialog window shown in Figure 226. Notice that voltages at each of the named nodes are automatically supplied, as is the current at the DC supply (VCC.i).

The data from the current probe, ICC.i, is redundant in this case. The numbered nodes are used to store information for DC back annotation, discussed in the section on Device Model RF Verification.

Figure 226. Insert Plot Dialog Box

Figure 227 shows there is good agreement between simulated and measured results. Measured data may be read in to ADS from either data files or instruments by selecting **Window>New File/ Instrument Server**. ADS will convert files in Touchstone, MDIF, Citifile or ICCAP formats to ADS datasets, which can then be displayed alongside simulated results. The I-V curves clearly show that, at the specified operating point of VCE=1V, ICE<0.6mA, the device will be operating in a low current regime. If designers do not have measure datafile, this step can be omitted.

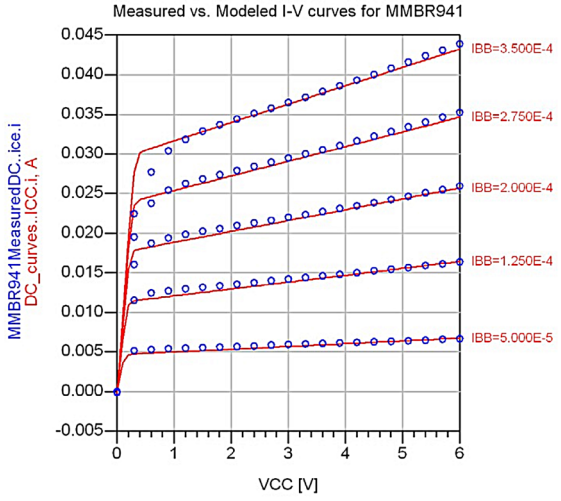


Figure 227. Comparison of Measured (symbols) and Simulated (Solid line) DC I-V Curves for MMBR941

Bias Network Design (Cell: BiasPoint)

The next step, selecting the device operating point and calculating the required bias resistors, is done using the set-up in BiasPoint.dsn as shown in Figure 228. Since the collector voltage and current have been specified, only the base current needs to be determined. In the schematic, VCC is fixed at 1V and IBB is swept from 1uA to 10uA, using the DC controller.

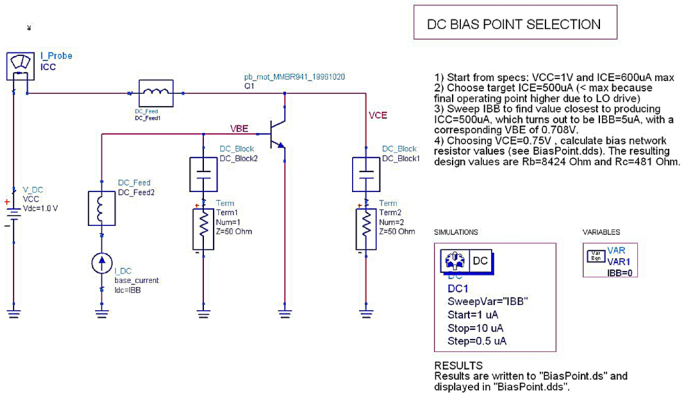


Figure 228. Calculation of Bias Point

The schematic contains bias tee components (the DC_Feed and DC_Block components) and 50-ohm terminations that mimic the actual test setup used to measure the device. However, since the DC simulation does not include any RF signals, they are not necessary at this point, and can be omitted without changing the results. The results are displayed in tabular format in BiasPoint.dds (see Figure 229), so the appropriate base current can be selected. Note that the bias point current is actually lower than the specified final value. This is because the device will be pumped with a relatively large LO signal, causing a shift in the DC component of the collector current.

This shift will be calculated more precisely later on but, for now, IBB is selected to be 5uA so that the corresponding collector current (514uA) is well below the specification.

Table 1: ICE and VBE vs. IBB, VCC=1V

IBB	BiasPoint..ICC.i	BiasPoint..VBE
1.000E-6	102.7 uA	665.5 mV
1.500E-6	154.5 uA	676.2 mV
2.000E-6	206.3 uA	683.8 mV
2.500E-6	257.9 uA	689.6 mV
3.000E-6	309.4 uA	694.4 mV
3.500E-6	360.8 uA	698.5 mV
4.000E-6	412.2 uA	702.0 mV
4.500E-6	463.4 uA	705.1 mV
5.000E-6	514.6 uA	707.9 mV
5.500E-6	565.7 uA	710.4 mV
6.000E-6	616.8 uA	712.7 mV

Sweeping IBB shows we need IBB=5uA to have ICC~=500uA. The corresponding VBE is 0.708V.

Figure 229. Device Operating Point Selection

The bias resistor values, shown in Figure 230, are calculated next. Base current, collector current and VCC are known, but the designer must make an assumption about the voltage drop across Rc to be able to solve for Rc and Rb. In this case, a collector-emitter voltage of 0.75V is chosen, providing a reasonable working voltage at the output and realizable resistor values. The equations, written in the data display page, calculate the exact values required for each value of base current, but of course the nearest standard values must be chosen. The next step is to confirm bias operation using these standard values and then verify the S-parameters of the model against measured values.

Table 2: Calculated Rb and Rc

IBB	Rb	Rc
1.000E-6	84529.635	2410.638
1.500E-6	49209.429	1602.222
2.000E-6	33115.916	1200.472
2.500E-6	24143.233	960.191
3.000E-6	18520.552	800.304
3.500E-6	14716.285	686.232
4.000E-6	11998.583	600.741
4.500E-6	9976.677	534.280
5.000E-6	8424.296	481.125
5.500E-6	7202.032	437.642
6.000E-6	6219.680	401.408
6.500E-6	5416.501	370.749

Eqn Rb= (0.75-VBE)/IBB

Eqn Rc=(0.25)/(ICC.i+IBB)

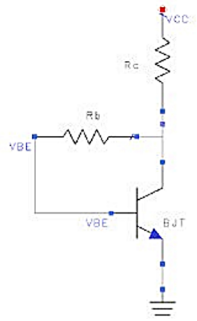


Figure 230. Calculation of Bias Network Resistors

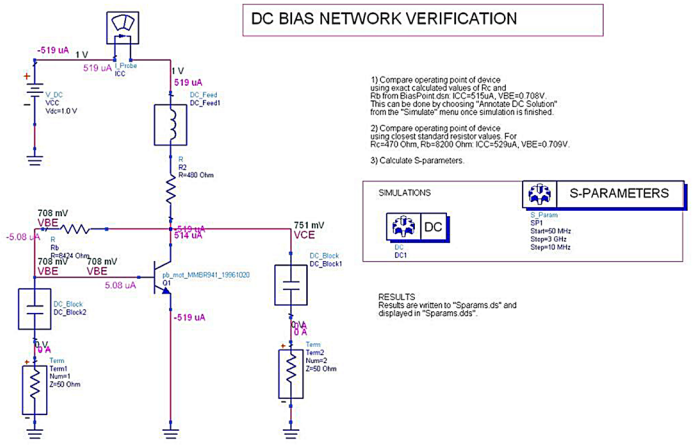


Figure 231. DC and S-Parameter Simulation Setup

Device Model RF Verification (Cell: BiasNet)

BiasNet.dsn, shown in Figure 231, includes both DC and S-parameter simulations so, in this case, bias tee components (DC feeds and blocks) are required to ensure proper RF performance. DC results are displayed directly on the schematic page, using the DC back annotation feature: once the simulation has been run, select Simulate>Annotate DC Solution to see the DC voltages and currents at each node. This simulation can be done with both the exact resistor values and nearest standard values (Rc=470 ohm, Rb=8.2 kohm) to confirm that the operating point is correct.

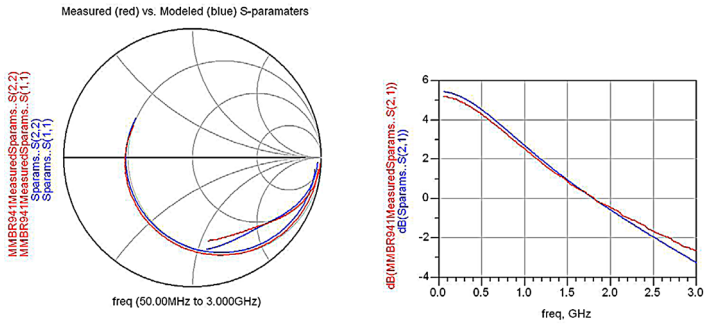


Figure 232. Comparison of Measured and Simulated S-Parameters for MMBR941

The device S-parameters are calculated at this operating point and displayed, together with measured data, in Figure 232. The good agreement obtained here verifies the small-signal RF performance. The device compression point will be simulated next to confirm large-signal operation.

Device Model Large-Signal Verification (Cell: Compression)

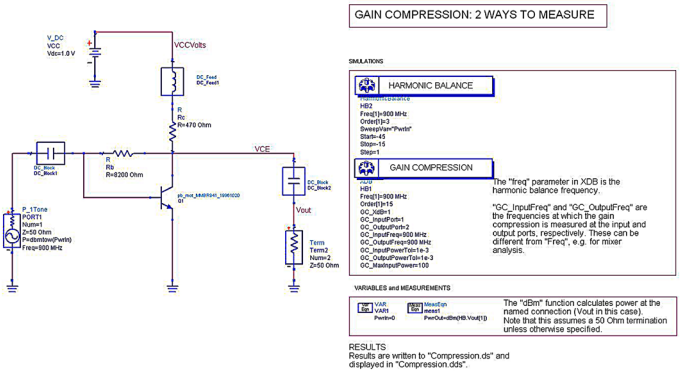


Figure 233. Device Compression Measurement Setup

Compression.dsn (Figure 233) shows two ways of calculating the device output compression at the RF frequency of 900 MHz. The conventional way, implemented here with the Harmonic Balance controller, is to sweep the input power level from low (i.e. small-signal) to high values until the output power compresses (the ratio Pout/Pin starts to fall off from its small-signal value). The input power variable, "PwrIn" is swept from -45 to -15dBm and a Measurement Equation component is used to define the output power at 900 MHz, in dBm. Notice that the dBm function assumes the power is being delivered to a 50-ohm load, unless otherwise specified by the user. The argument of the function, "HB.Vout[1]", specifies the fundamental frequency. Figure 234 shows the equation and graph used to determine the 1 dB compression point, and includes the measured results as well.

The second method, unique to ADS, is more direct and does not require graphs or sweeping variables. The Gain Compression controller "XDB" performs a harmonic balance analysis that correctly calculates and outputs the input and output power levels at the specified compression point. The default setting is 1 dB, but the user can specify any amount of compression. Figure 234 also shows the output from this method: the input and output power levels at 1 dB compression are listed in dBm.

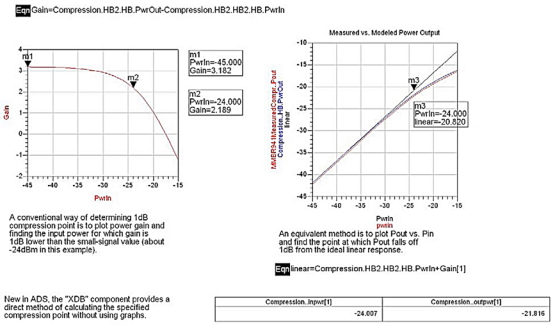


Figure 234. Two Methods of Determining 1 dB Compression - both show input P1 dB is -24 dBm

ADS offers a great deal of flexibility in where and how output data are defined. To take a simple example, “PwrOut” has been defined on the schematic page using a MeasEqn component, but it could equally well have been defined on the data display page as an equation. An advantage of defining outputs on the schematic is that they can be used in optimizations. On the other hand, defining them on the data display page is useful for setting up templates (where complex calculations can be easily applied to many different schematics). Also, any outputs that were overlooked before the simulation was run can be calculated afterwards by adding them on the data display page.

Notice that, at this point, the design still uses ideal bias tee components to isolate the DC and RF signal paths. These will be replaced with the real components that make up the matching networks in the next stage of the design.

Mixer Matching Circuit Design (Cell: RFIFmatch1)

An important step in mixer design is determining what impedances are seen at each port for both the RF and IF. The finished input network will match the device base to 50-ohms at the RF and present a short circuit at the IF (to prevent any noise at the input being amplified and interfering with the IF at the output). Similarly, the output network will match the collector to 50-ohms at the IF, while presenting a short circuit to the RF. Thus, for each frequency, the terminations seen at the input and output of the device are completely different. Since the device is not unilateral, the presence of a short circuit on one side of the device will affect the impedance seen at the other side for matching purposes.

The first step in designing the input matching network, then, is to determine the device input impedance at the RF when the output is terminated in a short circuit. For the output matching network, the designer needs to know the BJT’s output impedance at the IF when the input is terminated in a short circuit. In ADS, equation-based 1-port Z-parameter components are used to simulate this sort of idealized frequency-dependent termination, as seen in RFIFmatch1.dsn (see Figure 235).

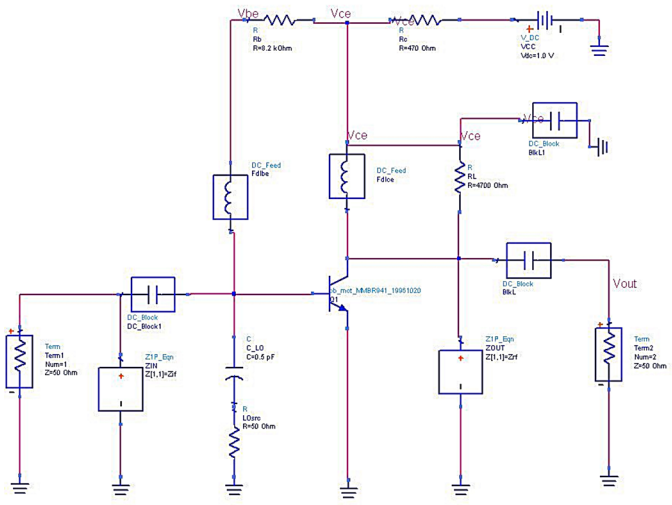


Figure 235. Calculating Device Impedance for Matching Network Design

The Z1P_Eqn components are defined in a VAR block. The one at the input, ZIN, is set to be a short-circuit at the IF and an open at the RF. This provides the required termination for S22 at the IF, while leaving S11 unperturbed at the RF. Similarly, ZOUT, at the output, is set to be a short at the RF and an open at the IF. Notice also that the LO source is represented at this point as an ideal 50-ohm termination, coupled to the mixer through a 0.5pF capacitor. The capacitor was chosen to be so small in order to isolate the LO source from the RF input signal. The return loss looking back through the capacitor towards the LO source is only 0.33dB at RF, so that it almost appears like an open circuit to the incoming RF signal. The penalty is that the LO, which is close in frequency to the RF, is also isolated from the circuit, meaning that a higher LO drive level is required. For example, when the LO source is set at -10dBm, only -22dBm reaches the mixer.

The resulting S-parameters at the RF show that the input impedance is (11.5 - j51.4) ohms with a short-circuit on the output. At the IF, the output impedance is (2065-j2010) ohms. These values can be used to decide on matching network topologies and component values. The designer always has several topologies to choose from in developing a matching network, and which one is best will depend on factors such maximizing yield (some topologies are more sensitive to component variation than others), minimizing component count (to reduce cost) and combining functions where possible (incorporating the bias decoupling components into the matching, in this case).

To illustrate, Figure 236 shows that, starting at the device input impedance (A), a shunt inductor followed by a series inductor will move the circuit impedance successively from B1 to 50-ohms. The resulting network “A” has some advantages: the shunt inductor will provide a short to the IF at the input, as required, and it can be used in the bias decoupling network (to replace the ideal DC_feed). However, network “B” is even better: using a smaller value of shunt inductance brings the impedance to B2, where a match is achieved using a series capacitor. C2 can also serve as the DC blocking capacitor, thereby saving a component, so this network is used for the mixer. *ADS provides an easy to use interactive Smith Chart tool utility that can be used for designing Matching Networks.*

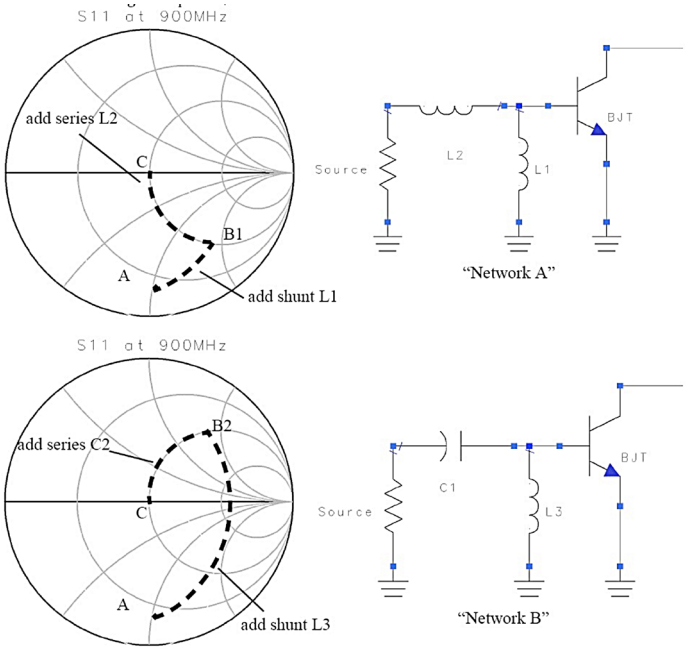


Figure 236. Choosing an Input Matching Network Topology

The output matching network was developed using a similar approach: starting from the Smith Chart, a matching network consisting of a shunt inductor followed by a series capacitor was designed. However, this topology would result in any RF at the output being dumped to the load instead of being short circuited as intended. To solve this, the shunt inductor (originally nearly 910nH, a very high impedance at RF) is replaced by an equivalent parallel LC combination. The capacitor must be large enough to provide a near-short for the RF, and a value of 33pF is chosen. The shunt inductor is then decreased, so the total reactance provided by the LC pair at the IF is the same as that of the original inductor.

Although it was not done in this example, the actual component values for the network can be calculated using ADS, as illustrated in examples like */examples/MWCkts/ LNA_1GHz_prj*. In this case, components were calculated manually from the Smith Chart, and the resulting circuit is shown in LOdrive.dsn. The final matching networks are shown in Figure 237. Notice that, in addition to components for the matching and bias networks, a load resistor, RL has been added to control the mixer's conversion gain. The initial value of 4.7 kohm was chosen to be high enough not to have an effect on the mixer's performance, and will be adjusted as required once the conversion gain is known. Also, two large RF bypass capacitors (BlkL1 and BlkL2) are added to provide RF ground to the output load resistor and inductor and to the input shunt inductor, respectively.

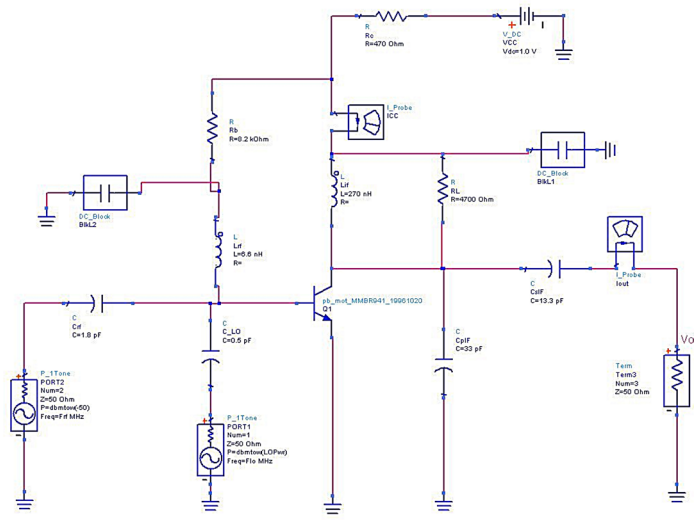


Figure 237. Mixer Matching Networks

Mixer Conversion Gain Versus LO Drive Level (LOdrive.dsn)

LOdrive.dsn (Figure 238) shows how to simulate conversion gain for the mixer and how to determine the effect of LO drive level on gain and DC bias. The RF and LO frequencies and the LO power level have been defined as variables. The RF drive level is specified at -50 dBm, while the harmonic balance controller is set up to sweep the LO drive level from -30 to -5 dBm. (The controller has many parameters, and the user can control which are visible on the schematic by editing the component and choosing the "Display" page in the edit dialog window). A simulation measurement equation defines the output power, in dBm, at the IF. Defining it here instead of the data display page makes it possible to optimize for output IF power, if needed. The "mix" function will return the component of the Vout spectrum defined by {-1, 1}, meaning {-Freq[1]+Freq[2]} or -LO+RF= IF (45MHz).

The P_IF equation calculates the dBm value of the mix function.

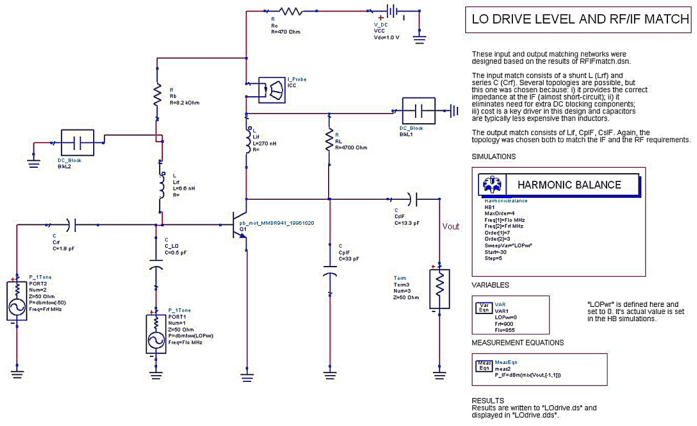


Figure 238. Set-up for Swept LO Drive Level Mixer Simulation

The data display shows the effect of the load resistor (Figure 239).

Since the conversion gain is the difference between P_IF and the RF, and the RF power is fixed at -50 dBm, the conversion gain can be calculated with a simple expression. Note that the default dataset, LODrive, contains results for a 4.7 kohm load resistor, and the conversion gain for this simulation is calculated by the equation "ConvGain". The conversion gain for a -10 dBm LO drive is 17 dB, which is unacceptably high. A second simulation was run with the load resistor reduced 1.5 kohm, which creates a lossy mismatch on the output. The results for that simulation were output to dataset LOdrive15, and equation "ConvGain_Rl5kOhm" shows the conversion gain is reduced to 13.7 dB. This is still higher than the specification of 10 dB, but will be left at this value for now since conversion gain can be expected to decrease further when non-ideal surface mount components replace the ideal components.

The second graph in the data display shown in Figure 239 illustrates the effect of the LO drive level on DC bias. Increasing the LO signal at the base drives the output swing on the collector harder, shifting the DC component higher (see Figure 240). In practice, a 5 to 15 percent shift in collector bias current typically gives good performance for a mixer of this type.

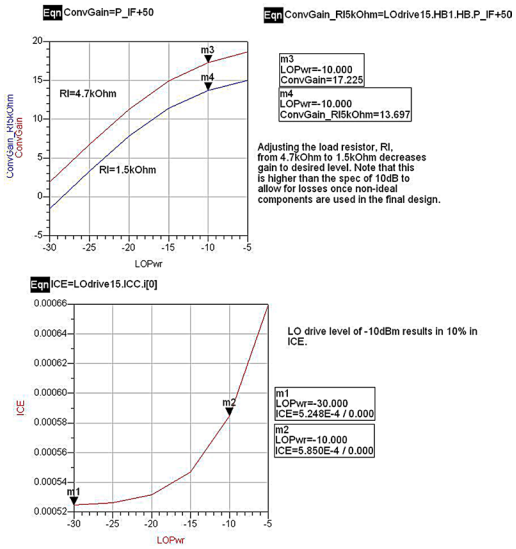


Figure 239. Conversion Gain and Bias Current Vary with LO Drive Level

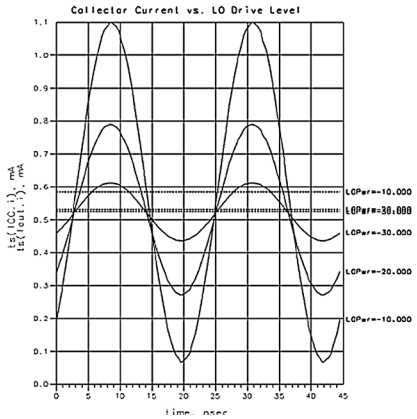


Figure 240. Variation in Output Collector Current with LO Drive Level

Mixer Conversion Gain Versus RF Signal Level (Cell: MixCompr)

The set-up for measuring mixer compression used in MixCompr.dsn is very similar to LOdrive.dsn except that the LO power level is now held constant at -10 dBm, while the RF power is swept from -50 to 0 dBm. As the results in Figure 241 show, the mixer's conversion gain reaches 1 dB compression at an input signal level of -27 dBm.

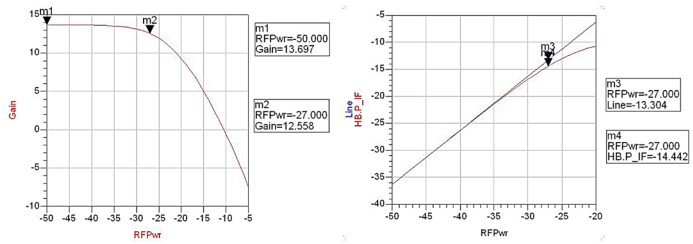


Figure 241. Mixer Conversion Gain Compression

Now that the mixer's performance is verified, the next step is to replace the ideal passive components with realistic models of the surface-mount resistors, capacitors and inductors that will be used in the actual circuit.

Creating the Mixer Layout (Cell: MixerLayout)

The design file MixerLayout.dsn contains a layout as well as a schematic. There are many possible ways to create layouts, and the best method will depend on the application. In this example, the first step was to convert all the components in the schematic to their nearest equivalent SMT part from the Passive Component Library. Next, these parts were placed in the layout window in their approximate locations. Interconnects were made in the layout window using the Trace command or microstrip components, and the final positioning of the components was adjusted. Finally, the schematic was updated using the design synchronization function.

MixerLayout.dsn was created by saving MixCompr.dsn under a new name and modifying it. Since the finished circuit will be simulated using the layout representation, it will have to be placed as a subnetwork in another schematic. This is because the layout file cannot contain simulator controllers, sources or terminations. The first step is to remove those components from the schematic and add ports to each point in the circuit that will be connected externally, either to sources, grounds or other circuits. The labels for each port will appear on the schematic symbol used when the design is placed in another schematic, so meaningful names should be provided. At this stage, the designer may also create a custom symbol for the circuit by selecting **View>Create/Edit Schematic Symbol**.

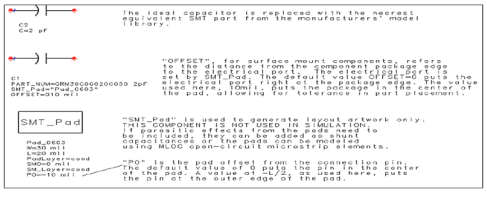


Figure 242. Substitution of SMT component for ideal component requires use of SMT_Pad

The next step is to replace each resistor, capacitor and inductor with a model of the SMT component that will be used in the actual circuit. The models are all found in the SMT Component Libraries by selecting the Browse and Search function in the Component Library List window. In this case, all the capacitors are MuRata Erie parts: the matching and bias capacitors are all MuRata Erie series GRM39 parts, while the RF bypass capacitors are GRM36 series. The resistors are taken from the Dale CRCW series and the inductors are Coilcraft parts. Where possible, parts are chosen to have a standard 0.060"x 0.030" footprint, although the inductors and RF bypass capacitors have different dimensions. Note that each SMT component specifies the name of the SMT_Pad component it uses. This SMT_Pad defines the pad-size to be used in layout, as shown in Figure 242. The designer must define these on the schematic page to ensure the pads appear correctly in the layout. Since each user will define the pads to suit their own board-fabrication process, the models do not include pad parasitics.

Once the components are placed and the pads defined, the designer can select **Layout>Place Components** from Schematic to Layout and place each part in its approximate location in the layout window. Traces are a convenient way to create the interconnects. They can be converted to equivalent microstrip components using the **Edit>Path/Trace/Convert Traces** command. In general, when moving back and forth between the schematic and layout representations, it is best to work on small sub-sections and synchronize the two representations manually. Synchronization ensures that both layout and schematic describe the same circuit: for example, if the designer has made some changes to the layout, the schematic can be updated to reflect them by selecting **Schematic>Generate/Update Schematic** in the layout window. Changes made to the schematic can be similarly transferred to the layout by choosing Layout>Generate/Update Layout in the schematic window.

Figure 243 shows the finished layout. A ground-plane has been added to the top-side metallization to eliminate the need for vias, thus reducing fabrication costs. This can be easily created in ADS by drawing a rectangle the size of the final circuit board and using the Edit>Create Clearance feature to generate the required spacing around transmission lines and component footprints.

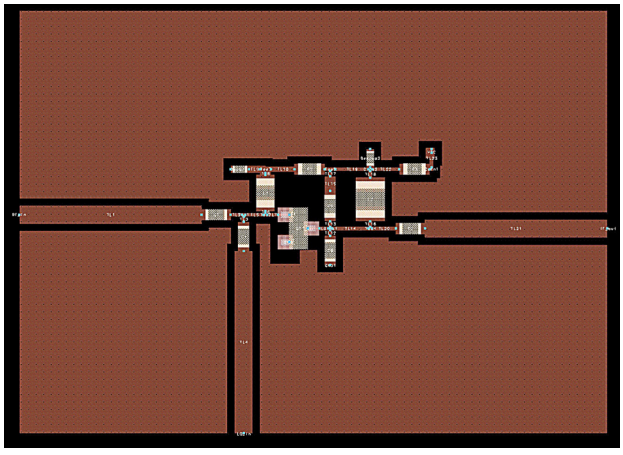


Figure 243. Finished Layout for Mixer Circuit

Finally, in this example the design will be simulated from layout, so the "SimLay" option is selected in the **File > Design/Parameters** dialog box. This allows the designer to see the effects of changes in the layout directly, without having to re-enter parameters in the schematic. Notice that components in the schematic can be modified (or even deleted entirely) without affecting the simulation, as long as the layout remains intact. Simulation from Layout (SimFromLayout.dsn)

SimFromLayout.dsn contains MixerLayout, together with the simulation controller, sources and terminations required to simulate it. The simulation setup is identical to the one used in LOdrive.dsn so the results using the non-ideal components may be compared directly. MixerLayout uses microstrip lines, so an "MSub" component is also included (Figure 244).

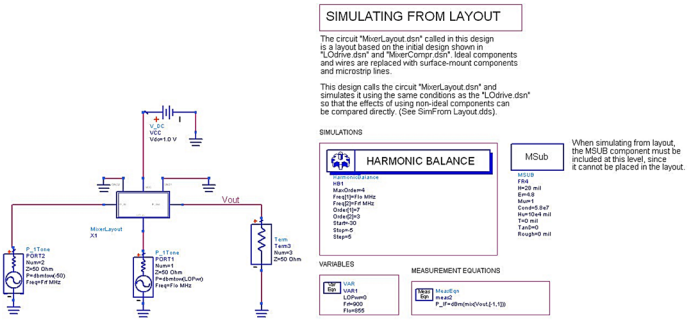


Figure 244. MixerLayout called as a sub-network in SimFromLayout.dsn

Figure 245 shows the mixer conversion gain as a function of LO drive level when simulated using both the ideal components and the SMT model components. As expected, the conversion gain has drops significantly, due mainly to the resistive losses in the inductors. This can be verified by replacing individual components with their ideal counterparts and re- simulating. The load resistor can now be adjusted to compensate for these losses:

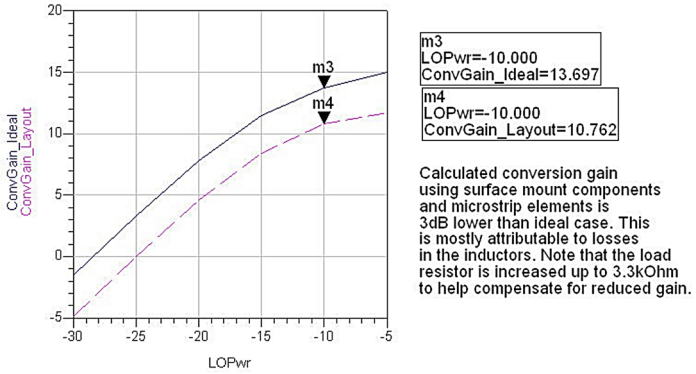


Figure 245. Comparison of Mixer Conversion Gain Using Ideal and SMT Components

Changing Rl from 1.5 kohm to 3.3 kohm restores the simulated conversion gain to 10.76 dB, providing a 0.76 dB margin over the specification. Note that these changes must be made in the layout file in order to be reflected in the simulation results. Once any such final corrections have been made to the layout, the circuit board is ready to be exported for fabrication.

Summary

An example mixer design using Keysight ADS has been presented, including details of the design process and simulation set-ups. This example is included with Keysight ADS and can be readily copied and modified by users for their own projects.

Additional Information on Mixer Design

Additional material and various Mixer design examples can be found at the Keysight EEsof EDA Knowledge Center:

http://www.keysight.com/find/eesof-knowledgecenter

Microwave Oscillator Design (1 GHz VCO)

Included with permission from the original author J.P. Silver. Original Author: J.P. Silver, E-mail: john@rfic.co.uk

ADS Licenses Used:

1. *Linear Simulation*
2. *Harmonic Balance*

Abstract

This paper discusses the design of a basic feedback oscillator, using a lumped element resonator with varactor control. A center frequency of 1 GHz has been chosen, with a tuning bandwidth of 50 MHz (i.e. 10% or 5.5 MHz/V) and a required phase noise performance of better than –70dBc/Hz at 10 KHz offset.

Introduction

This tutorial describes the design of a 1 GHz feedback oscillator building on the theory from the oscillator basics tutorial. Throughout the design Keysight ADS circuits and simulations are given to verify each design stage and show the predicted performance.

Lumped Resonator Design

Normally simple two-element resonators provide a zero phase shift while 4 element resonators such as the one shown in Figure 246 provide a 180-degree phase shift. The additional 180° phase shift in a microwave oscillator is usually provided by a length of transmission line used to complete the closed loop that is

$$\frac{c}{f} = \lambda_{air}$$

$$\therefore \text{Required transmission line length (180 degrees)} = \frac{\lambda_{air}}{2\sqrt{\varepsilon_r}}$$

where ε_r = the effective dielectric constant of the material.

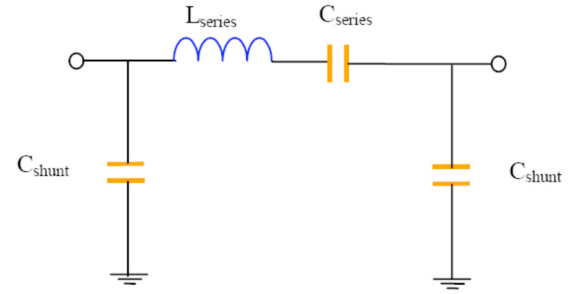


Figure 246. Element lumped resonator. The L-C series elements determine the resonant frequency of the oscillator and hence the oscillating frequency.

The shunt capacitors are required to set the loaded Q of the resonator to at least 15 to ensure a compliant phase noise response.

Effective capacitance which resonates with the series inductor L_{series} is :-

$$C_e = \frac{1}{\frac{1}{C_{series}} + \frac{2C_{shunt}(\omega_0 R_0)^2}{(\omega_0 R_0 C_{shunt})^2 + 1}}$$

R_0= input/output load resistance

Required inductance to resonate at f_0 is given by: -

$$L_{series} = \frac{1}{\omega_0^2 C_e}$$

We can now calculate the circuit elements required to form the resonator using the equations above. If for example we require a phase noise of say –70 dBc/Hz at 10 KHz (using a narrow-band (~50 MHz) VCO frequency of 1 GHz) we can use the ADS simulation shown in Figure 247 to find out the Loaded Q we require.

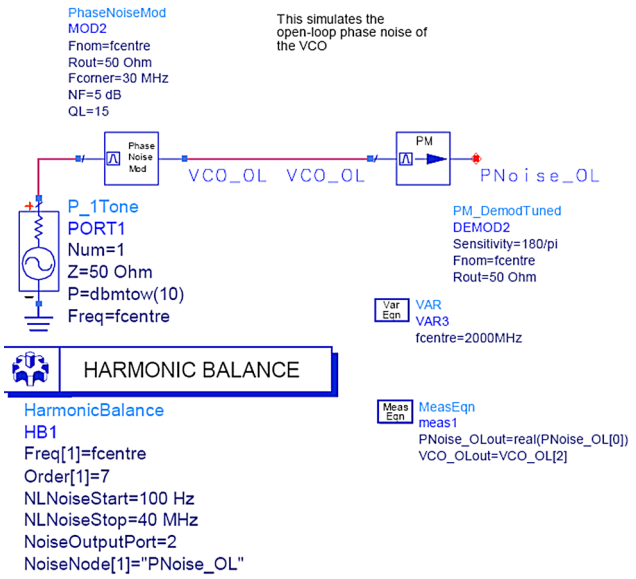


Figure 247. ADS simulation used to 'predict' phase noise performance given the resonator loaded Q, NF, Flicker corner frequency, center frequency and output power.

From the resulting simulation shown in Figure 248, we can see we require a loaded Q of greater than 15 to ensure a phase noise of –70 dBc/Hz at 10 KHz frequency offset.

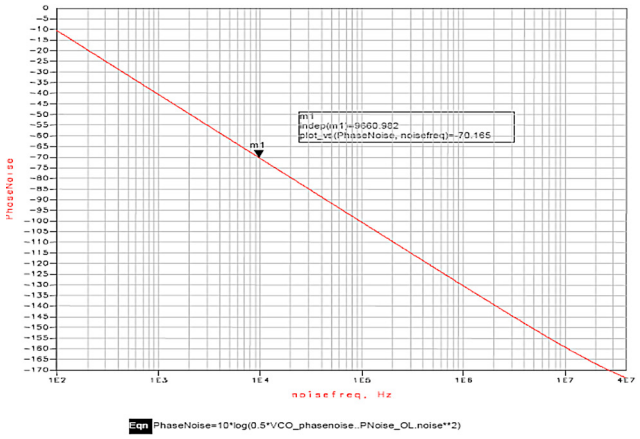


Figure 248. Resulting simulation from Figure 247 showing the resulting phase noise prediction with a marker set to 10 KHz frequency offset and VCO loaded Q to 15.

If we assume an unloaded Q of 120 for the inductor, therefore the effective Q,
Qe is given by : =

$$Q_e = \frac{1}{\frac{1}{Q_L} - \frac{1}{Q_U}} = \frac{1}{\frac{1}{15} - \frac{1}{120}} \quad 17$$

The required shunt reactance assuming an inductor value of 10 nH gives XL - $2\pi f$* 10-8 = 63Ω

$$X_{shunt} = R_o \left(\frac{2R_0 Q_e}{X_L} - 1 \right)^{-1/2}$$

$$= 50 \left(\frac{2 * 50 * 17}{63} - 1 \right)^{-1/2} = 9.8\Omega$$

$$C_{shunt} = \frac{1}{2\pi f X_{shunt}} = \frac{1}{2\pi * 1E^{9} * 9.8} = 16.2\text{pF}$$

Required inductance to resonate at f_o is given by : -

$$L_{series} = \frac{1}{\omega_o^2 C_e} \quad \text{therefore assuming}$$

$$L = 10\text{nH}\ C_e = \frac{1}{\omega_o^2 L} = 2.53\text{pF}$$

$$C_e = \frac{1}{\frac{1}{C_{series}} + \frac{2C_{shunt}(\omega_o R_0)^2}{(\omega_o R_0 C_{shunt})^2 + 1}} \quad \text{Re-arrange to get } C_{series} \text{ ie}$$

$$C_{series} = \frac{1}{\frac{1}{C_e} - \frac{2C_{shunt}(\omega_o R_0)^2}{(\omega_o R_0 C_{shunt})^2 + 1}}$$

$$= \frac{2 * 16.2E}{\frac{1}{2.53E^{-12}} - \frac{2 * 16.2E^{-12}(2\pi * 1E^{9} * 50)^2}{(2\pi * 1E^{9} * 50 * 16.2E^{-12})^2 + 1}} = 3.6\text{pF}$$

The calculated circuit element values for a 1 GHz resonator Q ~ 16 are shown in Figure 249.

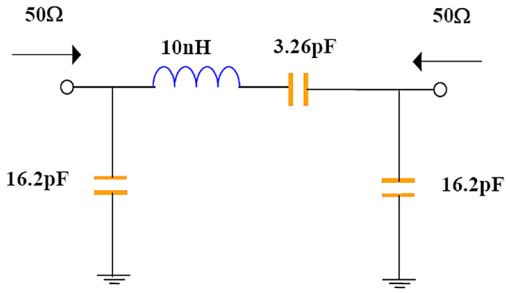


Figure 249. Final component values for the 4-element resonator designed to have a resonant frequency of 1 GHz with a loaded Q of > 15 in a 50-ohm system.

Figure 250 shows the ADS simulation setup for verifying the feedback filter network. Note that a 180-degree phase shift has been inserted to simulate the phase shift of the feedback amplifier described later. The output plot of this simulation showing amplitude, phase, group delay and loaded Q is shown in Figure 251.

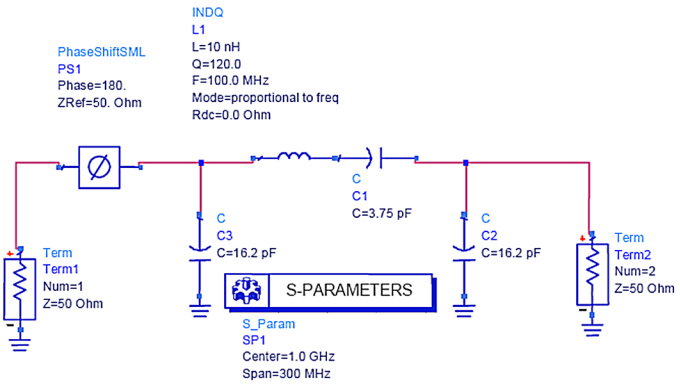
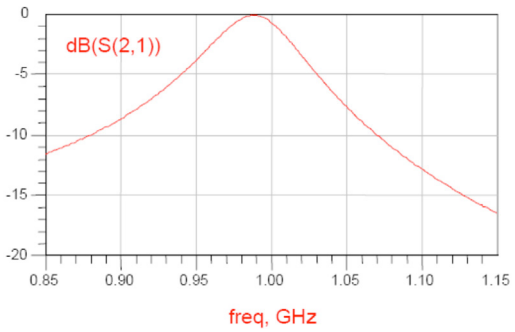
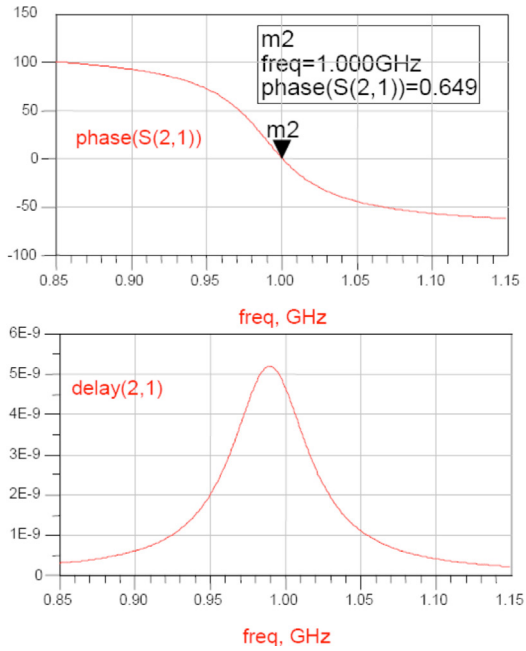


Figure 250. ADS S-parameter simulation for verifying the loaded Q of the feedback filter network.

The resonant frequency was slightly high so the series capacitor was increased from 3.26 pF to 3.75 pF. The measured Q from the plot was found to be ~16.2 (slightly off frequency – this can be adjusted later) i.e. within our specification. We now need what values of this capacitor we need (from a combination of the varactor and a varactor coupling capacitor) in order to give us our 50 MHz tuning bandwidth. It is easier to find this value by simulation, rather than trying to work back through the earlier equations. Using simulation, we find the capacitor value needs to vary from 3.4 to 4 pF.

For this design, the varactor chosen is the BB131. This has a capacitance of 11 pF at 1 V, 9 pF at 4 V and 3 pF at 10 V. To give us a capacitance swing of ~1 pF we need to add a series coupling capacitor of 3 pF. This will give us a combined capacitance of 2.25 pF at a control voltage of 4 V.





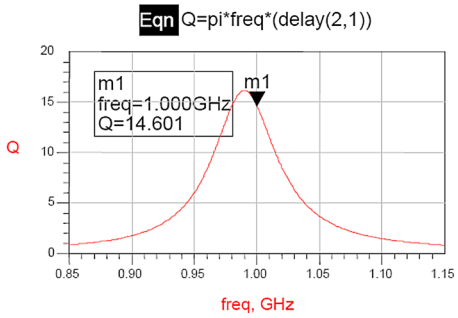


Figure 251. Simulation plot of the simulation of Figure 251, showing amplitude, phase, group delay and loaded Q. Loaded Q is > 15, slightly off frequency.

The data sheet of the varactor gives a series resistance (Rs) of 3 ohms at 470 MHz. We can therefore calculate the unloaded Q of the varactor:

$$Q_u = \frac{1}{2\pi.f.Rs.Vcap}$$

Where

Vcap = 6pF;Rs=3Ω&

f = 470MHz.

Therefore, $Q_u = 18.8$

To give us the correct resonant frequency another capacitor of 1.5 pF is connected in parallel with the varactor network as shown Figure 252. Note: ADS will scale the Q factor of the diode when simulating at 1 GHz even though the specified Q is at 470 MHz.

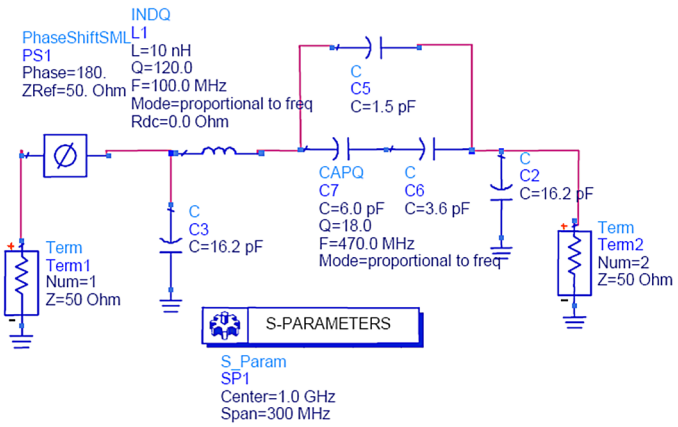


Figure 252. ADS simulation of the voltage controlled resonator. The varactor is given a Q of 18 at 470 MHz although ADS will calculate the Q at 1 GHz as part of the simulation.

The resulting Q plot of the above circuit is shown in Figure 253.

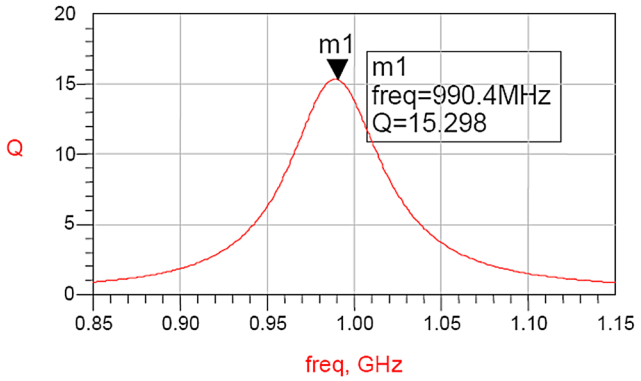


Figure 253. Q simulation plot with the varactor network and loaded Q of the varactor added to the simulation shown in Figure 252.

Feedback Amplifier Design

A suitable device to use as the feedback amplifier for this frequency is the Keysight AT-41486.

The data sheet shows that the unmatched gain at 1 GHz is quite high and therefore there is a possibility of instability. The main way of determining the stability of a device is to calculate the Rollett's stability factor (K), which is calculated using a set of S-parameters for the device at the frequency of operation. The calculations are involved and it is much quicker to simulate using ADS. To check the values of K, a simulation was run using the S-parameter model (8 V at 10 mA) with 50-ohm terminations. The ADS simulation for checking the stability factor (K) and maximum available gain (MAG) is shown in Figure 254. The tabulated results of the simulation are shown in the following table.

Note: For stability the Rollett's stability factor (K) must satisfy $K > 1$.

Clearly, in our un-matched simulation K is <1, showing that the device is only conditionally stable and may oscillate (without the resonator!) under certain source/load conditions.

There are a number of ways of increasing K to be >1 that all result in reducing the MAG. In this example, shunt feedback has been used to reduce the gain and increase stability with a view of making the amplifier unconditionally stable! However, we still need to ensure adequate gain margin is available as the resonator, when designed using 'real' component models, will be lossy.

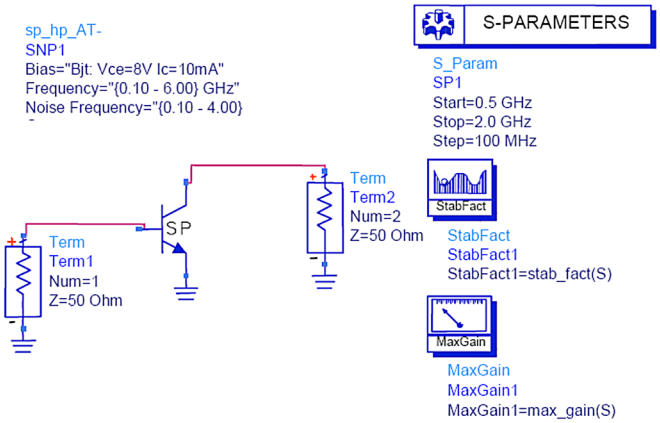


Figure 254. ADS simulation to determine the stability factor (K) and maximum available gain for the un-matched bipolar device.

freq	S(2,1)	StabFact1	MaxGain1
500.0MHz	12.630 / 1...	0.501	26.100
600.0MHz	11.488 / 1...	0.536	25.417
700.0MHz	10.346 / 9...	0.582	24.707
800.0MHz	9.204 / 93...	0.642	23.958
900.0MHz	8.062 / 88...	0.721	23.154
1.000GHz	6.920 / 84...	0.831	22.273
1.100GHz	6.480 / 81...	0.855	21.822
1.200GHz	6.040 / 78...	0.886	21.356
1.300GHz	5.600 / 75...	0.926	20.873
1.400GHz	5.160 / 72...	0.975	20.369
1.500GHz	4.720 / 69...	1.037	18.659
1.600GHz	4.498 / 66...	1.035	18.323
1.700GHz	4.276 / 63...	1.037	17.931
1.800GHz	4.054 / 61...	1.041	17.479
1.900GHz	3.832 / 58...	1.050	16.970
2.000GHz	3.610 / 56...	1.063	16.410

Stability factor (K) and maximum gain simulated results from the ADS simulation shown in Figure 254. At 1 GHz, K = 0.831 with a maximum associated gain of 22 dB.

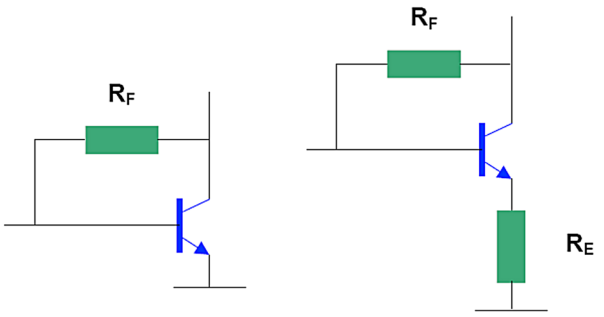


Figure 255. Topologies for broadband amplifiers, where feedback lowers gain but increases bandwidth.

The topologies for a broadband amplifier [1] using feedback to lower the gain and increase stability are shown in Figure 255. The design equations for calculating the bias resistors are shown below:

$$S_{21} = \frac{Zo - R_F}{Zo} \quad \text{Rearrange to get } R_F$$

$$R_F = Zo(1 + S_{21})$$

$$gm' = \frac{gm}{1 + gm.R_E} = \frac{R_F}{Zo^2}$$

$$RE = \frac{Zo^2}{R_F} - \frac{1}{gm} = \frac{Zo^2}{R_F} - re$$

$$re = \frac{1}{gm} = \frac{V_T}{I_E} \quad \text{Where } V_T = 25mV$$

Design for a gain ($S21^2$) of 10dB

$$S21mag = 10^{\frac{10}{10}} = 10$$

$$R_F = Zo(1+S_{21}) = 50(1 + \sqrt{10}) = 208\,\Omega$$

$$re = \frac{1}{gm} = \frac{V_T}{I_E} = \frac{25E^{-3}}{10E^{-3}} = 2.5 \quad \text{Where } V_T = 25mV$$

$$RE = \frac{Zo^2}{R_F} - \frac{1}{gm} = \frac{Zo^2}{R_F} - re = \frac{50^2}{208} - 2.5 = 9.5\,\Omega$$

The simulation for the small-signal feedback amplifier is shown in Figure 256, with the tabulated results shown in the following table.

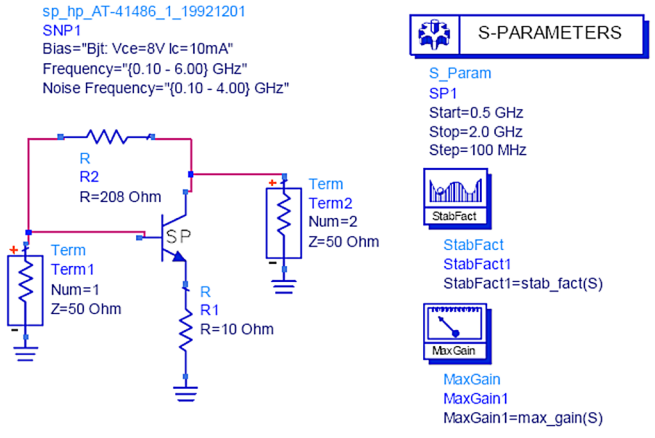


Figure 256. Small signal S-parameter simulation of the feedback amplifier circuit.

freq	S(2,1)	StabFact1	MaxGain1
500.0MHz	2.909 / 158....	1.159	9.366
600.0MHz	2.922 / 155....	1.156	9.430
700.0MHz	2.934 / 152....	1.153	9.501
800.0MHz	2.943 / 148....	1.151	9.576
900.0MHz	2.941 / 143....	1.149	9.644
1.000GHz	2.917 / 137....	1.148	9.683
1.100GHz	2.934 / 133....	1.141	9.817
1.200GHz	2.947 / 129....	1.132	9.959
1.300GHz	2.951 / 125....	1.121	10.108
1.400GHz	2.941 / 120....	1.108	10.262
1.500GHz	2.910 / 115....	1.091	10.418
1.600GHz	2.927 / 111....	1.063	10.758

Table of results for the feedback amplifier shown in Figure 257, showing the desired gain of 10 dB and a unconditionally stable design with K>1.

The feedback amplifier was then simulated using a SPICE model with its associated bias circuit as shown in Figure 257. The 190 ohm resistor was designed to drop ~ 2 V, so that ~ 10 V is applied across the emitter-collector junction as per the datasheet. The base bias of R3 & R4 was set up to ensure that 10 mA flows through the collector-emitter junction. To ensure that >10 dB gain was achieved R2 was increased to 360 ohms. The resulting table of results is shown in the following table.

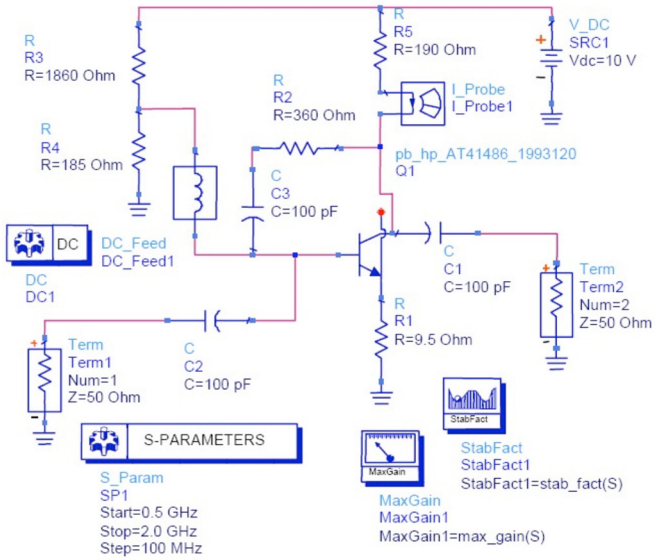


Figure 257. ADS simulation of the feedback amplifier using a AT41486 SPICE model. The 190-ohm resistor is designed to drop ~ 2 V so that ~ 10 V is applied across the emitter-collector junction as per the data sheet. The base bias of R3 & R4 is set up to ensure that 10 mA flows through the collector-emitter junction. To ensure that >10 dB gain was achieved R2 was increased to 360 ohms.

freq	MaxGain1	S(2,1)	StabFact1
500.0MHz	10.922	3.301 / 153.173	1.304
600.0MHz	10.782	3.244 / 147.097	1.324
700.0MHz	10.627	3.180 / 141.287	1.344
800.0MHz	10.464	3.112 / 135.704	1.364
900.0MHz	10.293	3.040 / 130.327	1.383
1.000GHz	10.119	2.966 / 125.144	1.398
1.100GHz	9.944	2.891 / 120.143	1.410
1.200GHz	9.770	2.816 / 115.315	1.418
1.300GHz	9.599	2.742 / 110.652	1.420
1.400GHz	9.431	2.669 / 106.144	1.418
1.500GHz	9.269	2.598 / 101.782	1.411
1.600GHz	9.113	2.529 / 97.559	1.399
1.700GHz	8.965	2.462 / 93.464	1.383
1.800GHz	8.824	2.398 / 89.490	1.363
1.900GHz	8.692	2.337 / 85.627	1.341
2.000GHz	8.569	2.278 / 81.869	1.317

I_Probe1.i
10.29mA

Results for the feedback amplifier shown in Figure 257. The table shows the desired gain of >10 dB and an unconditionally stable design with K>1. The current probe confirms the designed Ic of 10 mA.

Open Loop Analysis

With the feedback amplifier and resonator designed, the whole circuit can be simulated to check that at center frequency the phase is zero with ~10 dB of transmission gain.

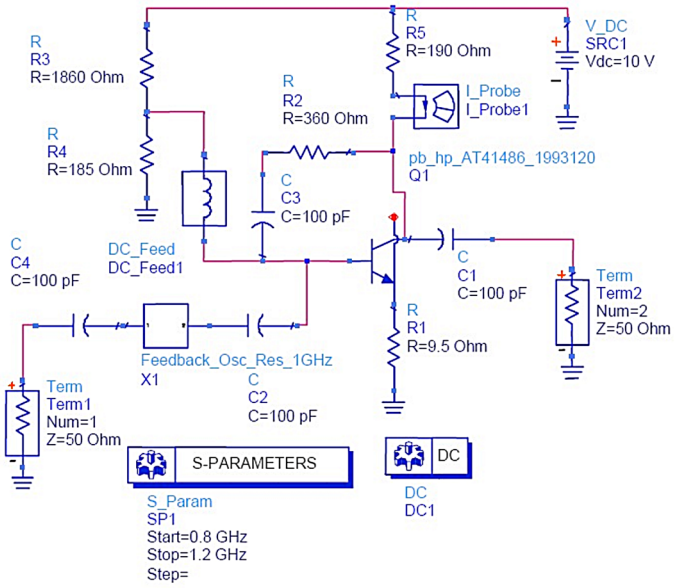


Figure 258. ADS open-loop simulation of the VCO, the sub-circuit of the resonator is shown Figure 259.

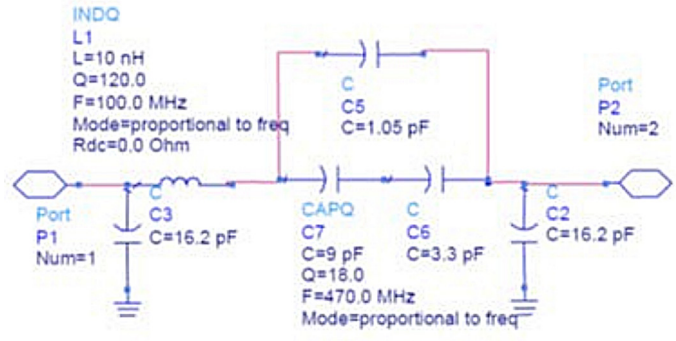
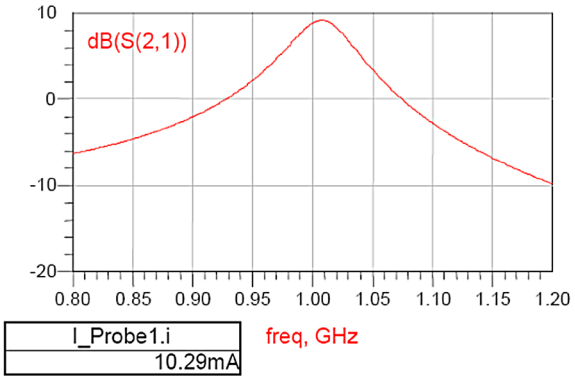


Figure 259. Sub-circuit showing the resonator section.

The resulting simulation plot of magnitude and phase at 4 V varactor control voltage is shown in Figure 260.



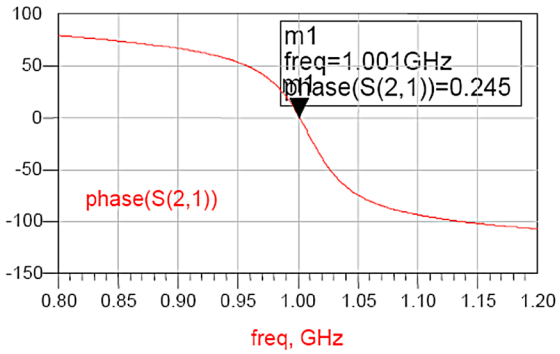


Figure 260. Results of the simulation shown in Figure 258. The insertion phase is zero degrees with a corresponding magnitude of ~ 10 dB. Therefore, the circuit should oscillate at 1 GHz.

Closed Loop Analysis

Small signal open-loop analysis is useful in checking that the resonator and amplifier are set at the correct frequency. However, when the loop is closed the amplifier will be forced into compression and as a result many of the RF parameters will alter, including the oscillating frequency. Performing a Harmonic Balance simulation of the oscillator will allow us to determine the operating frequency, output power, phase noise and harmonic levels.

The Harmonic Balance simulation for this VCO is shown in Figure 261 with the resulting plots of phase noise, output RF spectrum and oscillating frequency in Figure 263.

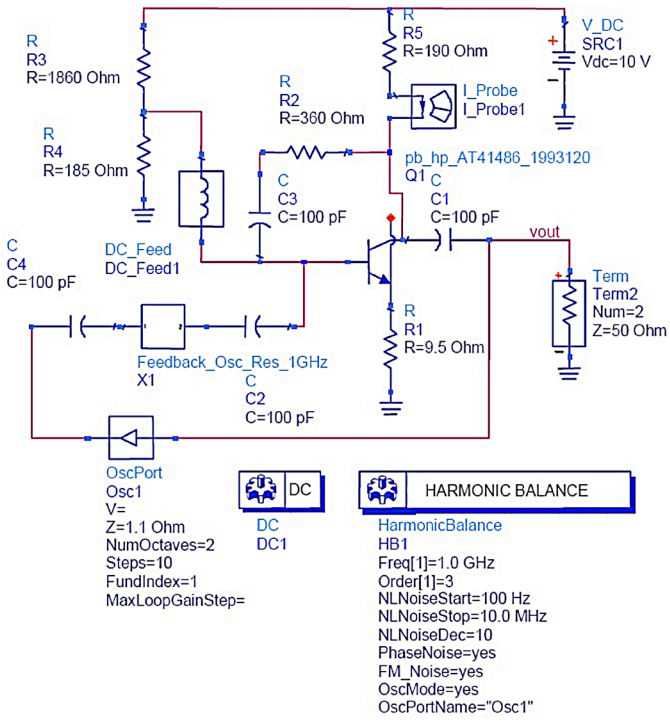


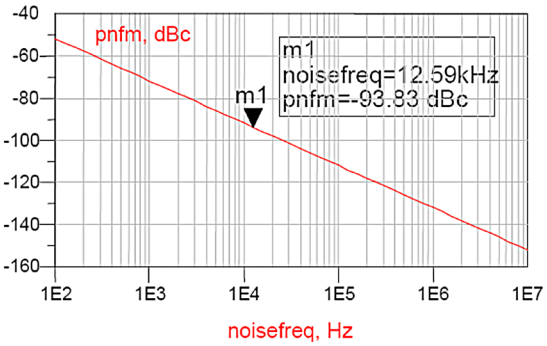
Figure 261. Harmonic Balance large-signal closed-loop simulation of the VCO. Note the output port is given the node name “vout” and must be entered in the harmonic balance setup on the “noise(2)” section.

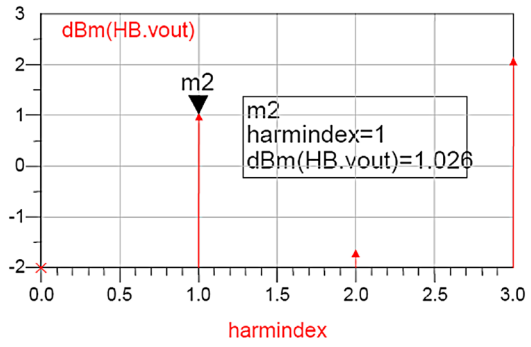
Note the frequency has shifted from that estimated in the open-loop simulations as a result of large signal effects of the transistor. The resonator requires some "tweaking" to bring it back on frequency and simulations performed at the maximum and minimum varactor control voltages to determine the simulated tuning bandwidth.

Altering the varactor values (after resetting the center frequency) shows that the tuning bandwidth is too wide at ~ 160 MHz (see the following table).

Control V	Vcap	Freq (MHz)
1	11pF	985
4	9pF	1000
10	3pF	1147

First run tuning bandwidth of the VCO showing a value of ~ 160 MHz.





harmindex	HB.freq
0	0.0000 Hz
1	974.2MHz
2	1.948GHz
3	2.923GHz

Figure 262. Resulting simulation plots from the HB circuit shown in Figure 262, showing the phase noise performance of –93 dBc/Hz, with an output frequency of 974 MHz and an associated output power of 1 dBm. Note the frequency has shifted from that estimated in the open-loop simulations as a result of large signal effects of the transistor. The resonator requires some "tweaking" to bring it back on frequency.

In order to reduce the tuning bandwidth the coupling capacitor in series with the varactor diode needs to be reduced (it will be necessary to adjust the overall parallel capacitor to re-center the VCO center frequency).

By altering the values of the capacitors shown in the resonator circuit of Figure 263, the modified resonator design gives a narrower tuning bandwidth. This circuit has a tuning bandwidth of ~60 MHz.

A summary of the simulated VCO frequency with varactor control voltage is shown in the following table.

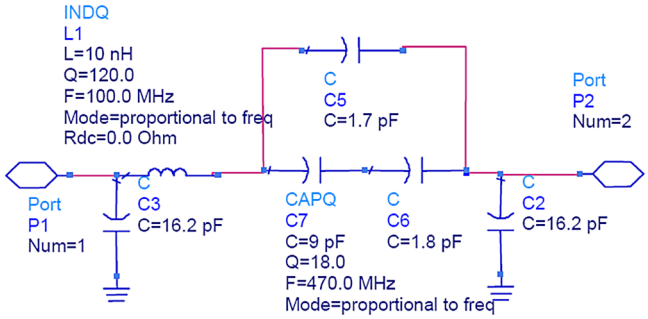


Figure 263. Modified resonator designed to give a narrower tuning bandwidth. This circuit has a tuning bandwidth of ~60 MHz.

Control V	Vcap	Freq (MHz)
1	11pF	995
4	9pF	1002
10	3pF	1055

Tuning range of the modified VCO with control voltage.

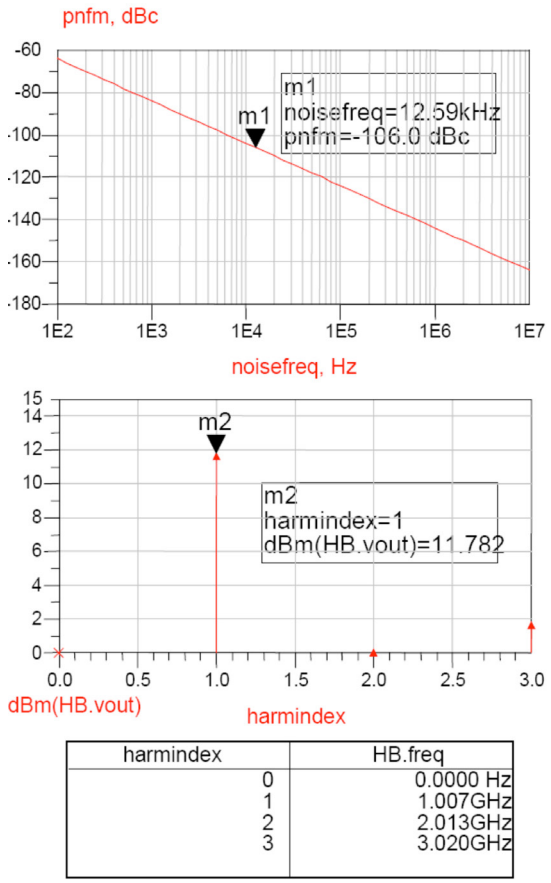
Simulations so far have shown that the RF output power is quite low at ~ 0 dBm. Examination of the circuit shows that at the moment we have large 100 pF capacitors connected to the 50-ohm load. This will cause large loading of the loop resulting in a frequency shift and loss of power. Therefore, the 100 pF capacitors were reduced from 100 pF to 10 pF, to lighten the coupling to the 50-ohm load.

The simulation result of the modified circuit is shown in Figure 264. The VCO output power has now increased by almost 10 dBm.

The following table shows the predicted summary of the VCO design.

Parameter	**Result**	**Units**
Centre Frequency	1000	MHz
Tuning bandwidth	62	MHz
Ko	6.8	MHz/V
Power	152	mW
Voltage	10	V
Phase Noise @ 10KHz	-106	dBc/Hz
Output Power	11.78	dBm

Predicted Summary of the VCO design



harmindex	HB.freq
0	0.0000 Hz
1	1.007GHz
2	2.013GHz
3	3.020GHz

Figure 264. Simulation result of the modified VCO circuit with the coupling capacitors reduced from 100 pF to 10 pF. Also, the parallel varactor capacitor was increased from 1.7 pF to 1.95 pF.

Conclusion

This tutorial described the design of a simple voltage controlled oscillator using a lumped element filter as the feedback element. The design process began with a fixed resonator design, followed by the addition of the varactor and its associated padding network. With the resonator designed, the amplifier section was designed using resistive shunt and series feedback to ensure a stable amplifier design with K>1 at 1 GHz. The final stages of the design involved, open-loop small signal analysis, followed by closed-loop large signal Harmonic Balance simulations. These Harmonic Balance simulations allowed phase noise performance, tuning bandwidth, Ko, output power and harmonic levels to be simulated.

Additional Information on Oscillator Design:

Additional material and various oscillator examples can be found at the Keysight EEsof EDA Knowledge Center:
http://www.keysight.com/find/eesof-knowledgecenter

References

[1] Microwave Circuit Design, George D Vendelin, Anthony M Pavio, Ulrich L Rhode, Wiley-Interscience, 1990, ISBN 0-471-60276-0, Chapter 6.

[2] Oscillator Design & Computer Simulation, Randell W Rhea, Noble Publishing, 1995, ISBN 1-884932-30-4, p36, p191 – p211.

[3] Fundamentals of RF Circuit Design (with Low Noise Oscillators), Jeremy Everard, Wiley Interscience, 2001, ISBN 0-471-49793-2, p156 .

Power Amplifier Design

ADS Licenses Used:

1. *Linear*
2. *Harmonic Balance*
3. *Circuit Envelope*
4. *PTolemy*

Power amplifiers are an inherent part of a transmitting chain, which is required to boost the signal and overcome channel losses between the transmitter and receiver.

Power amplifiers are the prime consumers of power in a transmitter. Hence, during the design stage, designers need to consider the efficiency, which is the figure of merit for how well DC power can be converted to RF power (also known as Power Added Efficiency, or PAE). Also, notice that efficiency translates into either lower operation costs (e.g. cellular base stations) or longer battery life (e.g. wireless handheld devices such as a mobile phone). Linearity is another important aspect of PA design; it preserves the input and output power relationship to maintain signal integrity. The design of PAs often requires a trade-off between linearity and efficiency.

There are many texts available for power amplifier fundamentals and classes of operation. This chapter mainly provides guidelines for designing an RF power amplifier in a step-by-step manner.

Power Amplifier Design Case Study:

Parameters	Specifications
Centre frequency	1 GHz
Bandwidth	±50 MHz
Output power (PEP)	25 Watts
Gain	> 10 dB
Input/return loss	< -10 dB
PAE	> 50%
3rd order IMD	< -30 dBc

Power Amplifier Specification for Case Study

In this case study, we will design a PA with specifications as shown in the above table and use a GaN (Gallium Nitride) based FET RF3931 from RFMD (www.rfmd.com). Designers can obtain the transistor library of GaN components for ADS2011 (or later) by contacting their local RFMD representatives.

Non-Linear Model for Power Amp Design:

Having a verified non-linear model is essential for having a good start for PA designs. Designers should contact their respective device manufacturers to obtain a non-linear model for the device they are using in their designs.

There are various ways in which a vendor can provide a non-linear model to designers:

a. SPICE model: this can be easily imported into ADS.
b. Non-linear model card: vendors provide device parameters for standard model cards such as Curtice Cubic, Statz, BSIM, etc. These can be used directly in ADS.
c. Design Kit: these kits contain the non-linear models for devices. These are usually encrypted to protect the IP.

If a non-linear model is not available, there are a few alternatives that manufacturers can give to designers. They include:

a. Optimum Zin and Zout over the frequency range: A problem with this approach is that designers can only perform input and output matching network design for the mentioned impedances in the datasheet. Full non-linear characterization of a PA cannot be performed.
b. Measured Load Pull data: This file is better than Zin and Zout because it also allows designers to characterize output power, efficiency, IMD, etc. as long as these are included in the measured load pull file. Again, a measured load pull file provides additional data but still does not allow designers to perform all the characterization that may be needed.

If a non-linear model is not available:

1. **Keysight IC-CAP**: Designers can use software like Keysight IC-CAP to perform non-linear modeling themselves. Usually, IC-CAP is used with a rack of instruments that may be needed for respective measurements, but this approach requires a good understanding of semiconductor physics and device behavior. More information about IC-CAP can be found on **www.keysight.com/find/eesof-iccap**.
2. **X-Parameters**: Many vendors have started to provide measured X-parameter-based models. Designers can also measure their devices and create X-parameter models themselves. This technique is more suitable as this is purely based on measurement and does not require an understanding of semiconductor physics, etc. Accuracy of the modeling depends on the accuracy of the measurements, which is easier to control for most of RF/uWave test engineers. X-parameters can be extracted for any prebuilt amplifier, i.e. amplifier or mixer modules; these are called 50-ohm X-parameters. These kinds of models can be used for system level simulations and for accurately modeling the non-linearities of these components at the system level.

For devices, the X-parameters have to be extracted over an impedance range by using impedance tuners at the source and load along with the rest of the accessories for high power handling. A typical measurement setup for a high power X-parameter measurement is shown in Figure 265.

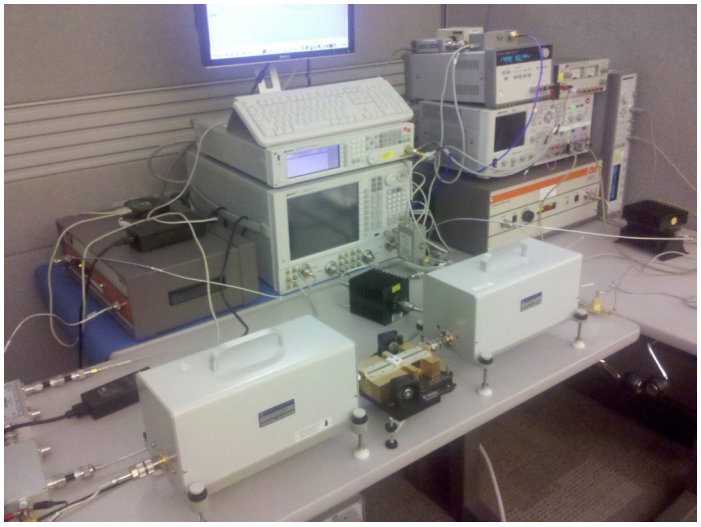


Figure 265. High Power X-parameter measurement bench

For more details on X-parameters, see: **www.keysight.com/find/nvna**.

In this case study, we have assumed that a non-linear model for the device is available for the designers.

Steps for Power Amplifier Design:

Key steps for designing a power amplifier are:

- DC and load line analysis
- Bias and stability
- Load pull analysis
- Impedance matching
- Source pull (optional step)
- PA final characterization – Did we meet the specification?
- Optimize/fine tune the design
- Test design with real world modulated signals (optional step)

Step 1: DC IV Characteristics

Create a new workspace in ADS. Make sure to include the lib.defs of the RFMD GaN library (or any other vendor for which a design kit is available) during or after the workspace is created. This will allow access to the non-linear models for devices like the RFMD RF3931, which is a GaN power device (**https://estore.rfmd.com/RFMD_Onlinestore/Products/RFMD+Parts/PID-P_RF3931.aspx?DC=25**). This device will be used for the amplifier design in this chapter.

a. Create a new schematic cell named “Step1_DCIV” and insert a DC IV template by going to **Insert->Template->FET Curve Tracer** as shown below.
b. Insert the RF3931 device from the RFMD library palette and modify the following parameters on the template:
    a. VDS=0 to 50 V in steps of 0.5 V
    b. VGS=-5 to 0 V in steps of 0.5 V

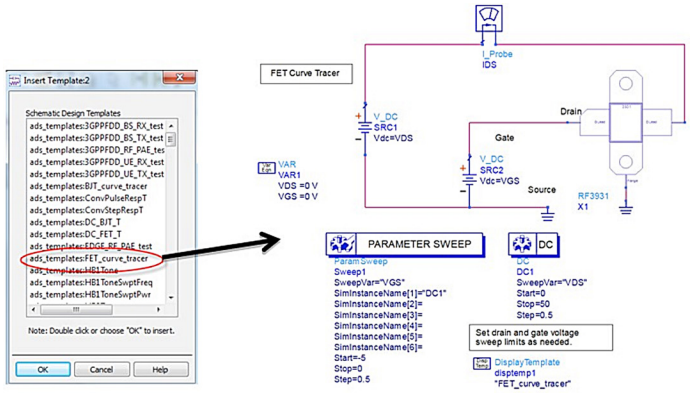


Figure 266.

c. Simulate the design and observe the data display where the IV characteristics of the device will be shown.
d. Do the following operations on the data display page:
   a. Insert 2 markers on the IV plot and place m1 and the IDSS point (close to peak current) and m2 marker near cutoff at Vgs=-5 V & VDS=50 V
   b. Using the Equation block, insert three equations on the data display to compute the load line:
      i. slope=(m1-m2)/(indep(m1)-indep(m2))
      ii. c=m2-slope*indep(m2)
      iii. Load_Line=slope*VDS[0,::]+c
   c. Double click on the graph, change the dataset to **Equations**, select **Load_Line**, then click on **>>Add>>** as shown here.
   d. Place marker m3 at VDS=48 V & VGS=-4 V and note the readout for DC power consumption. This is the bias that we will use for our PA for Class AB operation.
   e. Once finished, the data display page will look as shown below in Figure 268.

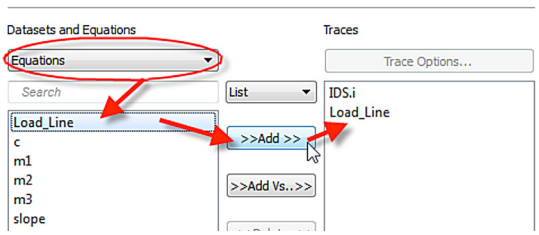


Figure 267.

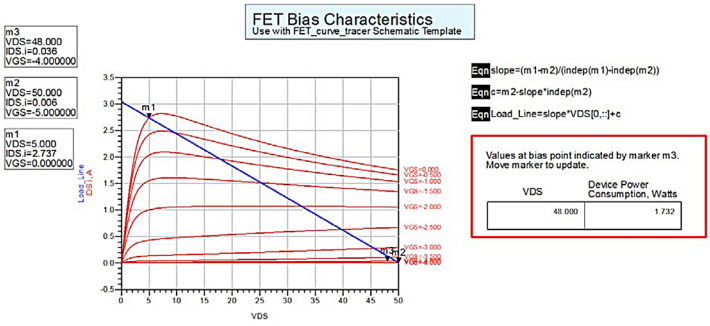


Figure 268. DC IV characteristics with Load Line.

Step 2: Bias Network Design:

Proper bias network design is essential for any non-linear circuit design. It is crucial to ensure that the right amount of bias reaches the device and does not load or leak RF energy. The choice of bias network topology is mainly dependent on the frequency of operation. For lower frequencies, designers can use inductors/chokes in the DC bias path; for higher frequencies, high impedance quarter wavelength lines are the preferred choice.

In the bias network design shown in Fig 270, various sections are marked, and zoomed views of each section are provided for easy understanding in Fig 270(a) – Fig 270(e). Open a new schematic cell named "Device_with_BiasNW" and place components as shown in the figure. You can also design your own bias network.

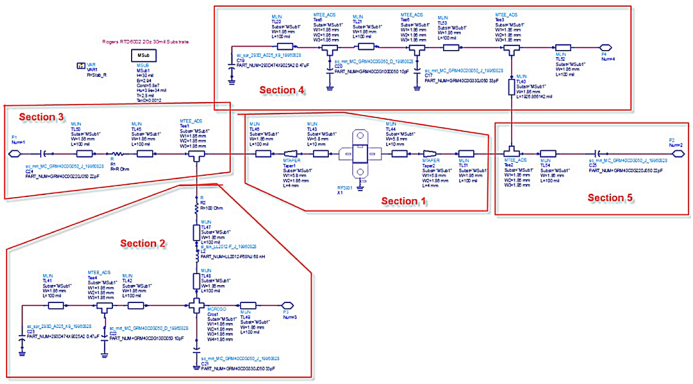


Figure 269. Bias Network for GaN power device.

From **TLines->Microstrip** library, place the MSUB component to define the parameters as shown below for the Rogers RTD6002 substrate. Define a variable as R=Stab_R, which shall be used for finding the required resistor value for device stabilization.

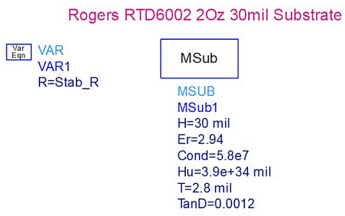


Figure 270.

Section 1: Device with terminal lead mounting lines and tapers to provide gradual transitions to the 50-ohm impedance lines. Microstrip line dimensions are shown in the snapshot below.

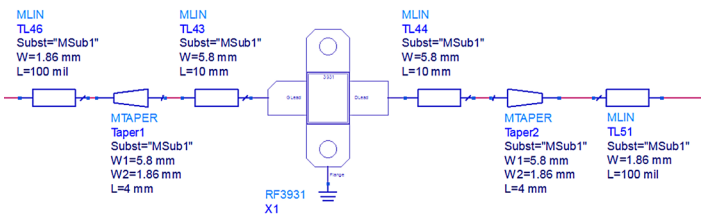


Figure 271.

Section 2: Gate bias section with three bypass capacitors, DC bias choke (inductor), and a 100-ohm stability resistor in series with the Gate bias.

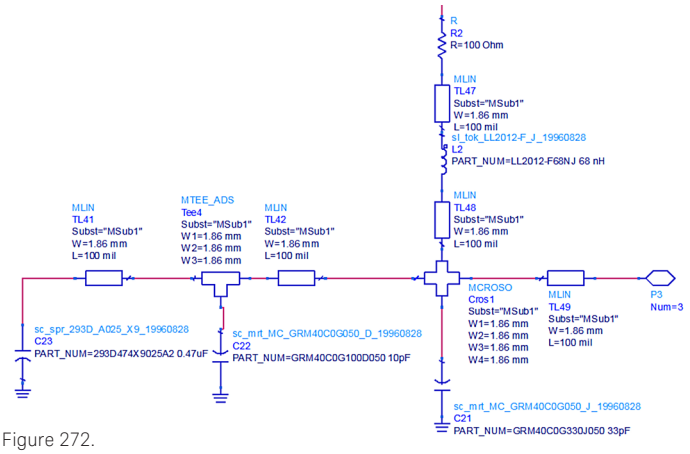


Figure 272.

Bill of Material for Gate Bias Section:

For SMT parts in ADS 2011, unzip the SMT components library (which can be found below) and add the **lib.defs** file from the unzipped folder to use the components in the design. Use **DesignKits->Manage Libraries** option in the ADS main window:

<ADS install dir>\oalibs\componentLib\RF_Passive_SMT_vendor_kit
e.g: C:\Keysight\ADS2011_10\oalibs\componentLib\RF_Passive_SMT_vendor_kit

Component name & type	Value	Library
C21 – SMT capacitor	33 pF	Murata: sc_mrt_MC_GRM40C-0G050_J_19960828
C22 – SMT capacitor	10 pF	Muratra: sc_mrt_MC_GRM40C-0G050_D_19960828
C23 – SMT capacitor	0.47 µF	Sprague: sc_spr_293D_A025_X9_19960828
L2 – SMT inductor	68 nH	Toko: sl_tok_LL2012-F_J_19960828
R2 – SMT resistor	100 Ω	Lumped components
Other microstrip lines	As shown in snapshot	TLines – microstrip

Section 3: Section 3 is for the input side of the bias network, which includes a resistor R1 for device stability. The value is defined as **R Ohm**, which we shall tune to achieve stability for the power device.

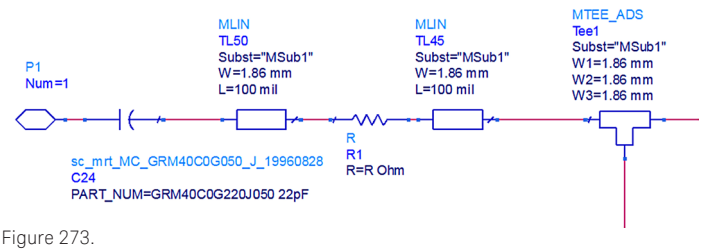


Figure 273.

Bill of Material for Section 3:

Component name & type	Value	Library
C24 – I/P coupling SMT capacitor	22 pF	Murata: sc_mrt_MC_GRM40C-0G050_J_19960828
R1 – SMT resistor	R Ω	Lumped components
Other microstrip lines	As shown in snapshot	TLines – microstrip

Section 4: This part of the bias network provides the bias to the drain of the device.

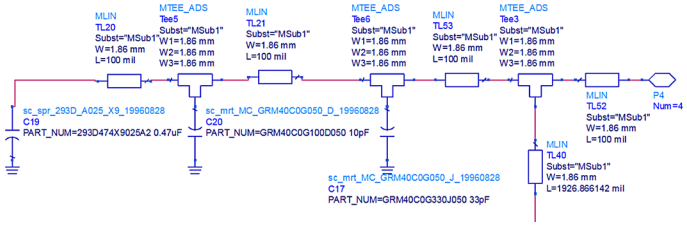


Figure 274.

Bill of Material for Drain Bias Section:

Component name & type	Value	Library
C17 – SMT capacitor	33 pF	Murata: sc_mrt_MC_GRM40C-0G050_J_19960828
C20 – SMT capacitor	10 pF	Muratra: sc_mrt_MC_GRM40C-0G050_D_19960828
C23 – SMT capacitor	0.47 uF	Sprague: sc_spr_293D_A025_X9_19960828
Other microstrip lines	As shown in snapshot	TLines – microstrip

Section 5: This part is for the output side of the bias network.

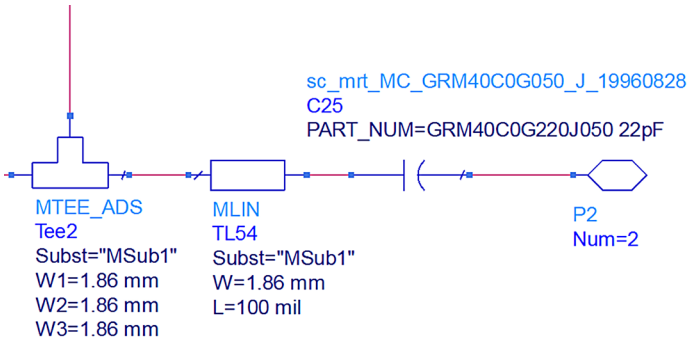


Figure 275.

Bill of Material for Section 5

Component name & type	Value	Library
C25 – O/P coupling SMT Capacitor	22 pF	Murata: sc_mrt_MC_GRM40C-0G050_J_19960828
Other microstrip lines	As shown in snapshot	TLines – microstrip

Hierarchal parameter definition for Stability resistor

We shall define a top level parameter for the stability resistor value to easily set it at the top level when we want to tune, optimize, or modify it to see the difference in results.

Go to **File->Design Parameters->Cell Parameters**, and enter the following:

Parameter Name: Stab_R
Default Value: 5
Parameter Type: Unitless
Parameter Description: Stab_R
Make sure the following boxes are checked:

a. Display parameter on schematic
b. Optimizable
c. Allow statistical distribution

Click on **Save AEL file** and click **OK**.

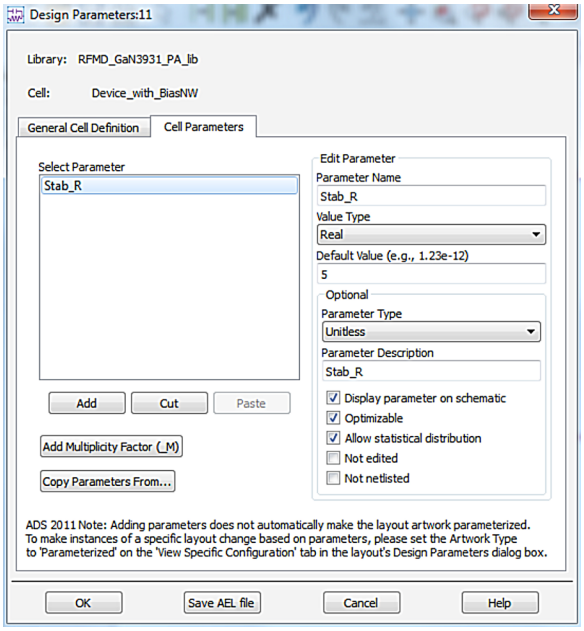


Figure 276.

Step 3: Small Signal Stability Analysis

Open a new schematic cell named "Step2_Small_Signal_Stability," and, from the main ADS window, drag and drop the design cell "Device_with_BiasNW." You will see a symbol generation message; click **Yes**, then **OK** on the symbol generator dialog to see a default symbol with four pins appear. From the workspace tree under the cell name, double click on **Symbol**. This will open the symbol editor to create our own symbol for better understanding and use in this workspace.

Create the following symbol using the symbol editor icons on the left hand side of the symbol generator schematic. Provide relevant text for easier identification of the connection pins. Note that ports 1-4 should be matching the names/places where ports are kept inside **Device_with_BiasNW**, e.g. Port 1 is connected at the RF input of the Gate terminal of the device as shown in the Section 3 snapshot earlier.

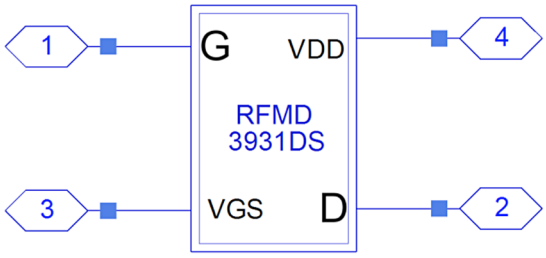


Figure 277.

Place the device on the schematic and create the stability analysis bench as shown below. Place StabFact and StabMes measurement components from the Simulation-S_Param library. Set Stab_R=10 so that the stability resistor value inside the subnetwork is set to 10 ohms.

Necessary and sufficient conditions for a stable device include: Stability Factor (K) > 1 and Stability Measure > 0

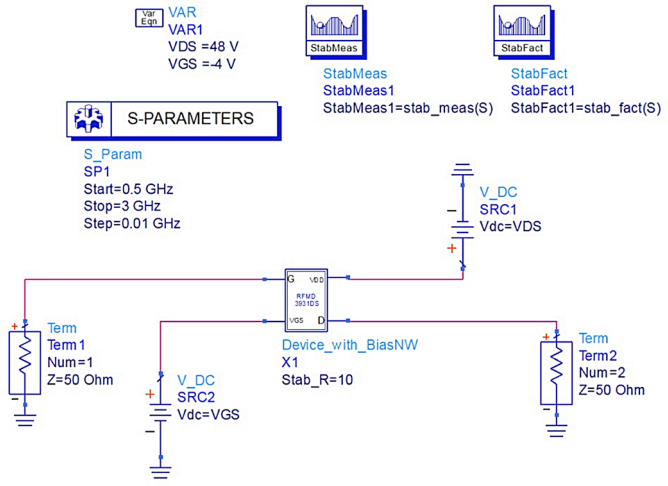


Figure 278.

Perform a simulation and plot the stability factor and the stability measure on the rectangular graph as shown.

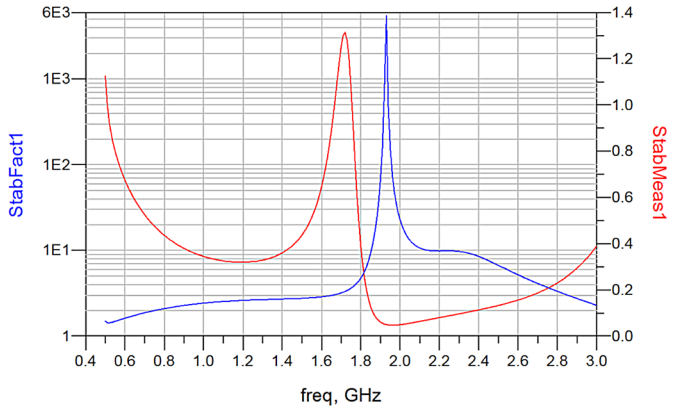


Figure 279.

In the graph shown here, the stability factor is plotted on the left Y-axis with a log scale, and the stability measure is plotted on the right Y-axis. As can be seen the stability factor is more than 1 and the stability measure is greater than 0 over the entire frequency range; hence our device is stable with the help of stability resistors inside the subnetwork. We can begin our actual PA analysis as outlined in the next few sections.

Step 4: Load Pull Analysis

Load pull is a very commonly used and preferred analysis for PA design applications. Load pull is the technique during which the source impedance and source power are kept at a constant level. Then the impedance or reflection coefficient of the load is swept over a certain section of the Smith Chart to characterize output power, PAE, IMD (with 2-tone Load Pull), etc. This yields the optimum impedance to be presented to the device. Next we perform impedance matching network design.

Critical things to determine while performing load pull simulations include:

a. Which section of the Smith Chart to use for the load impedance
b. What source impedance to keep while performing load pull simulations
c. How much source power is needed

There are no straight-forward answers to these questions, but one can follow simple guidelines as given here to work through them in an iterative manner before the final load pull analysis.

Tip 1: How to select the correct area in the Smith Chart for load pull

To determine which section of the Smith Chart to use, the device datasheet can provide certain information. A section can also be designed and various areas of the Smith Chart examined to finalized the optimum location. Usually, power devices work at lower impedances, so sections near the periphery are a good place to start. The Smith Chart can be divided into four quadrants to help determine the right area to zoom in and perform load pull simulations.

Tip 2: What source impedance to keep during load pull

Usually, power devices have lower impedances. Therefore, keeping the source impedance at 5 or 10 ohms offers a good starting point; this can then be tweaked to arrive at a better value. After a successful load pull simulation, ADS provides a good estimate of the optimum source impedance. Designers may also perform Source Pull analysis to find the optimum source impedance for maximum gain, hence reducing the compression level while extracting the required amount of output power from the device. For example, in our case we have used a 10-ohm resistor in series with the gate. Therefore, we shall keep 15 ohms as our starting point for the source impedance during our load pull simulations.

Tip 3: How much source power is needed

A good estimate of the source power can come from the device datasheet, which provides the gain of the device at a certain frequency. To calculate the required input power, use the formula = (output power required – gain as mentioned in datasheet) + 3dB. It can then be reduced or increased through a couple of iterations, and the final value of the source power can be decided.

Load Pull Simulation for our Amplifier:

1. Click on **Designguide->LoadPull->One Tone, Constant Available Source Power Load Pull**. This will copy a few schematics and a data display onto the workspace tree. Rename HB1Tone_LoadPull to **Step4_LoadPull** and HB1Tone_LoadPull.dds to **Step4_LoadPull.dds** as shown here:

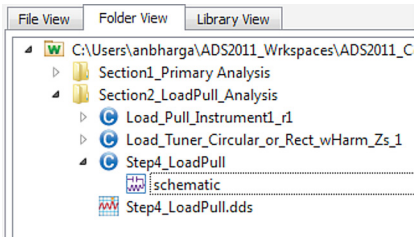


Figure 280.

2. Open the schematic of **Step4_LoadPull** to see a load pull instrument with a default device. Delete the device and its connections, then drag and drop **Device_with_BiasNW** onto this schematic. Set **Stab_R = 10** and make connections to the load pull instrument. Make the following changes on the parameters by double clicking on the load pull instrument:
   a. V_Bias1 = -4 V
   b. V_Bias2 = 48 V
   c. RF_Freq = 1000 MHz
   d. Pavs_dBm = 34
   e. S_imag_min = -0.3
   f. S_imag_max = 0.4
   g. S_imag_num_pts=10
   h. S_real_min = -0.9
   i. S_real_max = -0.3
   j. S_real_num_pts = 10
   k. Z_Source_Fund = 15+j*0

Once finished, the schematic will look as shown here:

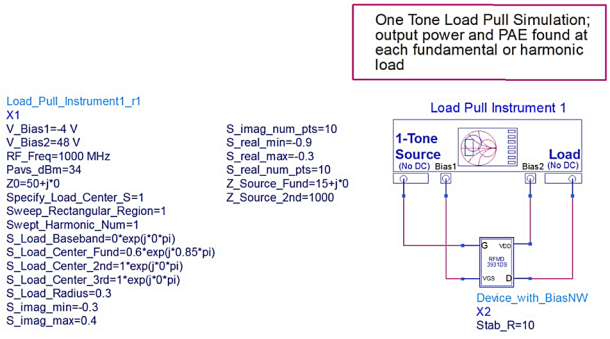


Figure 281.

Perform the simulation by clicking on the **Simulate** icon, or press **F7**. Observe the data display, which provides all the useful information.

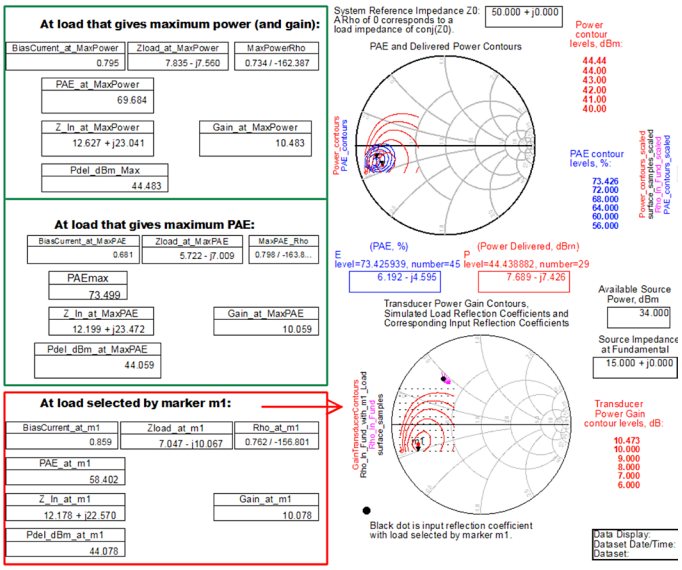


Figure 282.

Zoom to the section which shows **"At load that gives maximum power (and gain)."**

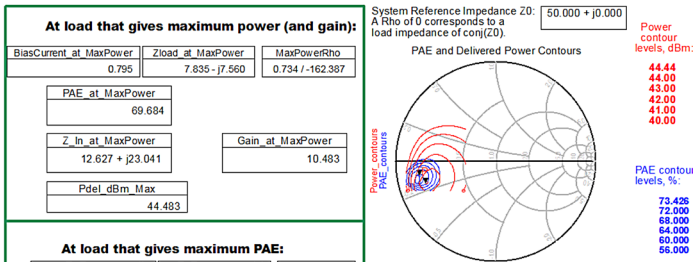


Figure 283.

Notice that we are able to achieve the required output power of 44 dBm (25 Watts), but the gain seems to be lower than what is mentioned in the datasheet (which should be more than 12 or so). This is because we have not yet terminated the source in its optimum impedance for maximizing the gain. We can note the optimum load impedance, which is shown as 7.835-j*7.56 ohms, and if we match our device to this load impedance, we shall obtain 44 dBm of output power.

Go to the schematic and modify the **Z_Source_Fund = 12.6 –j*23** (complex conjugate) as predicted by the load pull simulation, which is the right termination for the source. For a more sophisticated simulation, designers can use the source pull template provided in the Load Pull DesignGuide. With this method, we will terminate the load using the impedance of 7.835-j*7.56, then vary the source impedance to find the optimal termination. This provides the maximum gain from the device. For this exercise, we shall use the source impedance as computed by the load pull simulation.

Perform the load pull simulation again and observe the **Pdel_dBm_Max** and **Gain_at_MaxPower** as shown below.

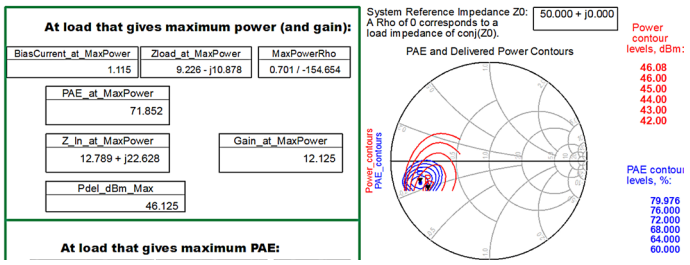


Figure 284.

We can observe that the output power has risen to 46 dBm, and gain has gone up to 12 dB. This indicates that we can reduce the input power level by 2 dB or so to achieve 44 dBm output power. Modify the source power **Pavs_dBm** to 32 and resimulate the design. Then observe the data display to note that we obtain output power of 44.75 dBm and gain of 12.75 with a PAE = 72%.

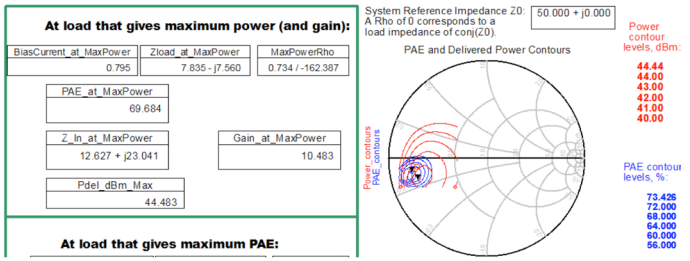


Figure 285.

Take away from our load pull analysis:

Input Source Power = 32 dBm
Input Impedance = 12.6 + j*23 ohms
Load Impedance = 7.835 –j*7.56 ohms

Step 5: Impedance Matching Network Design

ADS offers a variety of choices to perform impedance matching network design. Designers can choose any of the options listed below:

a. **Tools->Smith Chart**: This allows users to perform lumped element and transmission-line-based matching network design using an interactive Smith Chart tool.
b. **Tools->Impedance Matching**: This is a "smart component"-based impedance matching network synthesis that also allows users to perform broadband matching using lowpass, highpass or bandpass topologies. The default synthesized network is always lumped components. By using the lumped–to-transmission-line transformation, one can transform lumped components to equivalent transmission lines.
c. **DesignGuide->Passive Circuit**: This design guide can be used to synthesize single stub or double stub transmission-line-based matching networks.

Output Matching Network Design:

For the present case of a power amplifier matching network, we will use the Smith Chart tool in ADS, which provides greater control of the impedance matching network design.

1. Click on **Tools->Smith Chart** to see a pop up window of the Smith Chart.
2. Click on the **Smart Component Palette** icon to see the Smith Chart component in the Schematic palette as shown on the next snapshot.
3. Place the Smith Chart component on the schematic and select this component from the drop down box in the Smith Chart tool. **Uncheck the Normalize option**.

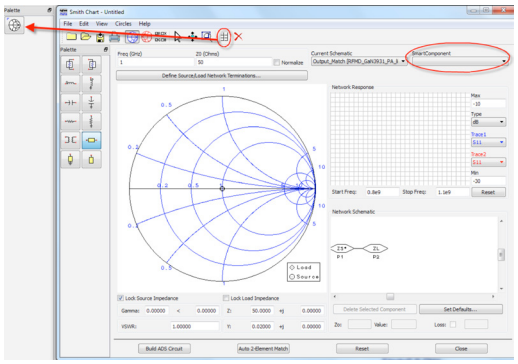


Figure 286.

4. Click on **ZS*** in the Network Schematic, then click on **Lock Source Impedance**. Select **ZL** and enter Z as 7.835 –j*7.56 as computed by our final load pull simulation. Once ZL is shifted to the desired impedance point, select **Lock Load Impedance** so that we don't disturb the impedance point by mistake. Once done, it should look similar to the one shown below.

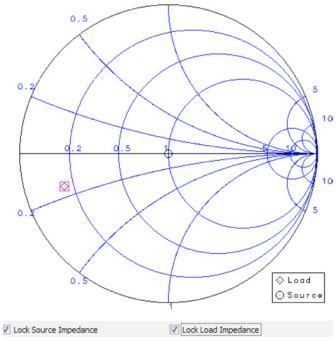


Figure 287.

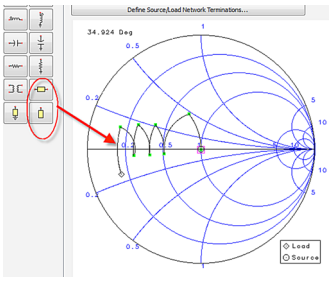


Figure 288.

5. Now, we are ready for impedance matching using either the L and C components or using the transmission lines in the component list.
   a. Click on **Series Line** and move your mouse over the Smith Chart; notice the locus point moving with your mouse in the upper direction, indicating series inductor action. The transmission line electrical length will be displayed in the upper left corner of the Smith Chart. Click the SmithChart once you approach 16.1 degrees.
   b. Click on the **Open Circuit** stub. Now the locus should move downwards, indicating a capacitive action. Left click once the length approaches 75 degrees.
   c. Repeat the series line and open stub three more times for the following lengths (as close as you can reach):
      i. Series Line 1 = 16.2 degrees
      ii. Shunt Stub 1 = 73 degrees
      iii. Series Line 2 = 11 degrees
      iv. Shunt Stub 2 = 58.6 degrees
      v. Series Line 3 = 13.2 degrees
      vi. Shunt Stub 3 = 46.5 degrees
      vii. Series Line 4 = 35.1 degrees
      viii. Shunt Stub 4 = 35 degrees
   d. The final snapshot will look similar to the one shown above. Designers can choose how many sections they would like to have in their matching network by taking slightly longer curves. However, the bandwidth and matching network would be more sensitive to process variation (remember Q-factor fundamentals). Designers can also plot Q-circles for matching network design by using the **Circles->Q** option of the Smith Chart tool.
   e. A larger matching network will consume more area on a PCB; hence a tradeoff between size and number of sections must be taken into account. Another trick to reduce the size of a matching network is to increase the impedances of series lines or reduce the impedances of shunt stubs. These actions will increase inductive and capacitive properties of the transmission lines, respectively.
   f. After this impedance matching network design, we have the ideal transmission line properties (i.e. impedances and electrical lengths for the matching network components). We can use LineCalc (Transmission Line Calculator) in ADS to compute the physical width and length of these lines based on the dielectric material, which is used for circuit design. Refer to some of the earlier chapters on how to use LineCalc in ADS.
   g. Remember that our source and load impedances used in the Smith Chart tool are actually reversed (we kept the source at 50-ohms and the load at 7.8-j*7.5). Therefore, we need to flip the output matching network when used with the device so that the source impedance is 7.8-j*7.5 and the load impedance is 50-ohms as actually required.

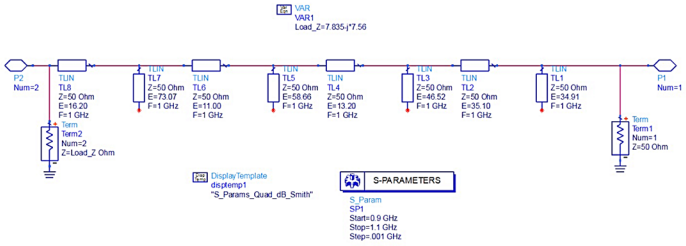


Figure 289.

Notice that the flipped network with the source impedance is defined as 7.835-j*7.56 and the load as 50-ohms (ignore the variable name that says Load_Z).

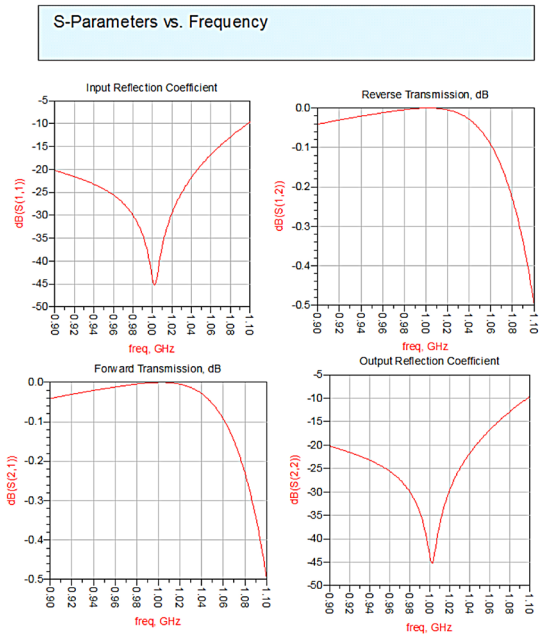


Figure 290.

Input Matching Network Design:

Similar to output matching network design, the input matching network can be designed with four series transmission lines and four shunt open circuit stubs. The Smith Chart display will look similar to the one shown below.

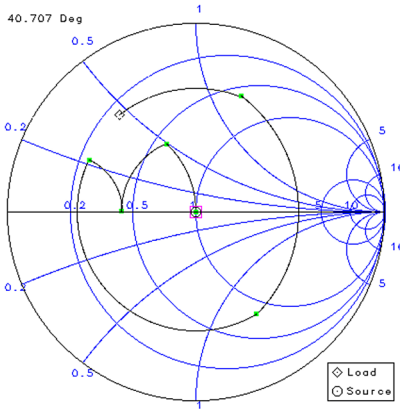


Figure 291.

i. Shunt Stub 1 = 40.71 degrees
ii. Series Line 1 = 32.83 degrees
iii. Shunt Stub 2 = 64.03 degrees
iv. Series Line 2 = 73.21 degrees
v. Shunt Stub 3 = 49.54 degrees
vi. Series Line 3 = 29.78 degrees

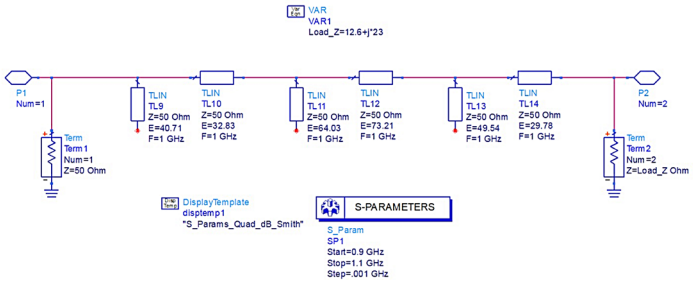


Figure 292.

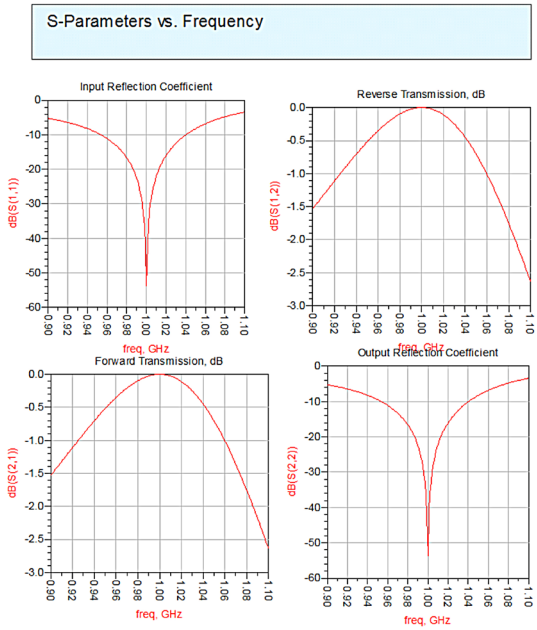


Figure 293.

Matching Network After Microstrip Line Transformation Using LineCalc:

Substrate definition and physical dimension calculation in LineCalc

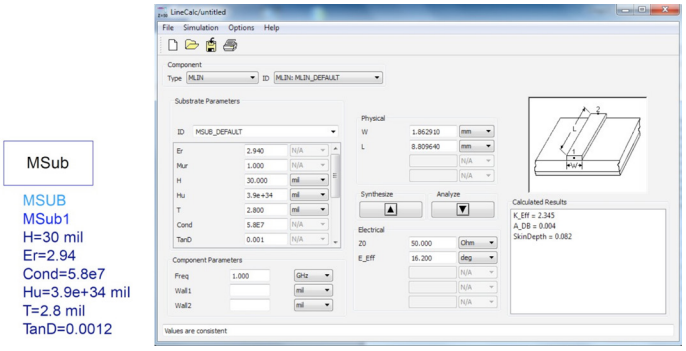


Figure 294.

Output Matching Network:

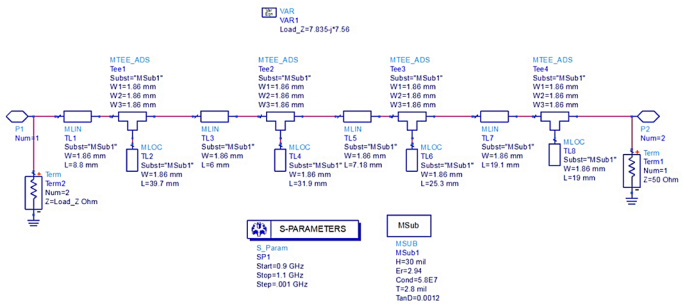


Figure 295.

Input Matching Network:

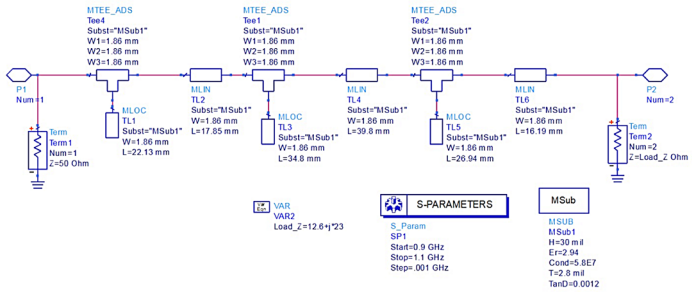


Figure 296.

Did we meet all amplifier specifications?

Create a new schematic cell with a name "**Step5_PA_with_Match**" and place **Device_with_BiasNW** (don't forget to set Stab_R=10) with input and output matching networks. Then, set up the 1_Tone HB simulation to see if we have met all the specifications as shown in the next snapshot.

The Current Probe component can be found under **Probe Components**, and the PAE function can be found under the **Simulation-HB** library. Also note that these probes have been renamed Iin, Iout, and Idc for easier identification, and vin, vout, and vdc node names (wire labels) have been provided for the PAE() function.

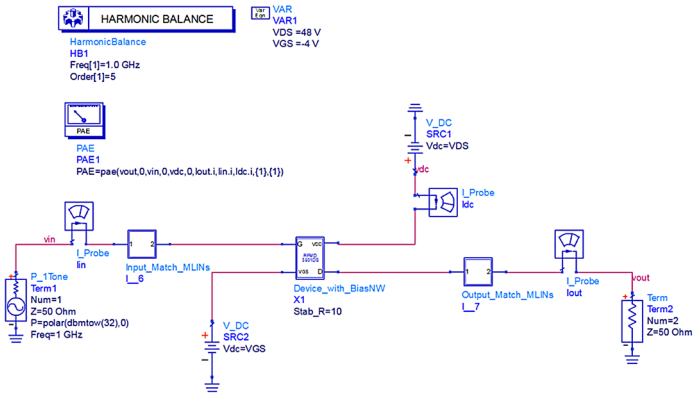
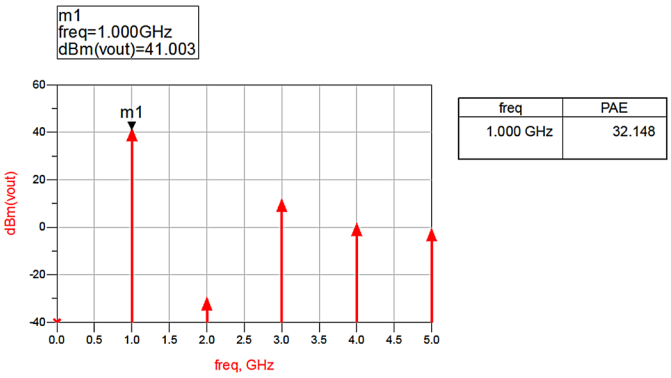


Figure 297.



freq	PAE
1.000 GHz	32.148

Figure 298.

From the above simulation, notice that the output power is 3 dB lower than expected. Also, the efficiency is much lower than our specification, and we will need to optimize the matching networks to meet our required specifications.

Step 6 - Power Amplifier Performance Optimization

1. Right click on **Step5_PA_with_Match**, click on **Copy Cell**, then select **Include Hierarchy** so that all subcircuits get copied along with the main design. Note that a "_v1" suffix will be added to all the designs as shown in the Copy Files window.

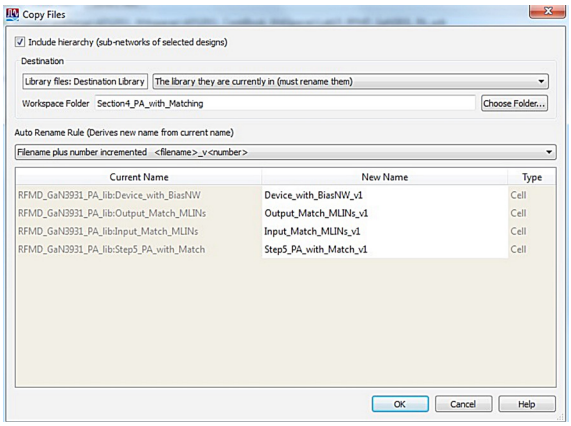


Figure 299.

2. Click **OK**, then notice the new design cells in the ADS main window. Right-click on **Step5_PA_with_Match_v1** and select **Rename**, give the new name as **Step5_PA_with_OptimizedMatch**, and double click its schematic to open it.
3. From the Opt/Stat/DOE library, place two Optimization Goals and an Optimization Controller.

   a. **Goal 1**: PAE (or PAE1) > 55 (our requirement is 50% but we will keep an extra 5% for better confidence).
   b. **Goal 2**: dBm(vout[1]) > 44.5 ("[1]" indicates the fundamental of the output power spectrum; our required power is 44 dBm but we will keep an extra 0.5 dBm for better confidence).
   c. **Optimization Controller**: Optimization Type: Gradient, Iterations: 200

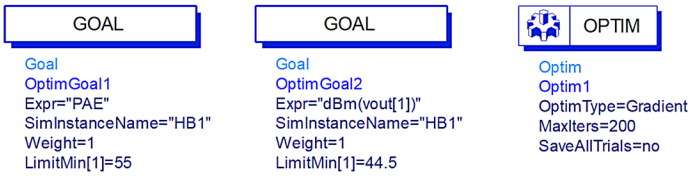


Figure 300.

Please note: by default you may not see LimitMin[1] as shown in the above two goals; this can be switched on by going to the display tab of the goals. Similarly, all other unnecessary items are switched off for the optimization controller.

4. Go to **Simulate->Simulation Variables Setup**.... and click on the **Optimization** tab in the pop-up window. From the input and output match subcircuit components, click on the transmission line lengths to make them optimizable. It is possible to optimize the widths as well, but in this case we will just optimize the lengths of the transmission lines. By default, the Min and Max for length will be +/-50% of the nominal value, which is sufficient for our purposes.

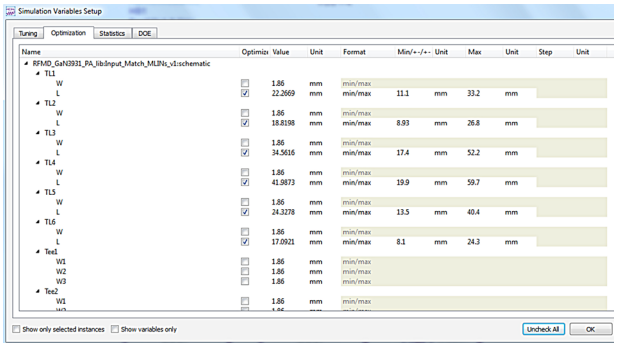


Figure 301.

Click **OK** once all parameters are defined as optimizable.

5. Click on the **Optimization** icon in the schematic to begin the optimization process. Once the desired goals are achieved, the Error will reach 0. This indicates that we have achieved our desired specifications.

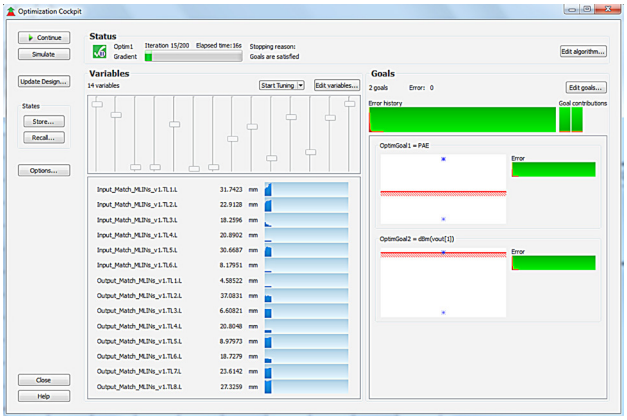


Figure 302.

Click on **Close** and select **Update the Design**. Perform the simulation by clicking on the **Simulate** icon on the schematic tool bar, then note the optimized results.

Optimized PA Response:

As we can see from the optimized results, we now meet the desired specifications of power and efficiency. We can go ahead and perform some additional simulations on our amplifier for complete characterization as illustrated in the next few sections.

1-Tone Power Sweep Analysis:

1. Define a new variable, e.g. pin=32
2. In the **P_1Tone** source, define "pin" instead of 32 so that the input power can change once we sweep the pin variable.
3. Double click on the **HB controller** and go to the **Sweep** tab; define the following:
   a. Parameter to Sweep = pin
   b. Start = 28
   c. Stop = 34
   d. Step-size = 0.2
4. The overall setup should look similar to the one shown in the next snapshot.

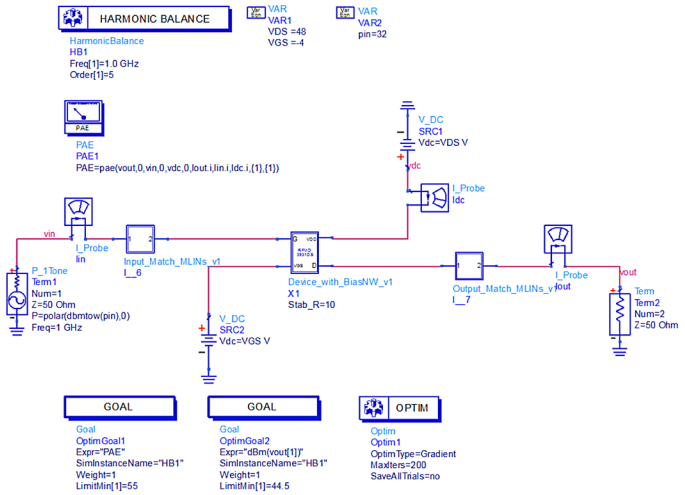


Figure 303.

5. Click on the **Simulate** icon to simulate the design. Spectral lines with various arrows indicate output power in each frequency component (i.e. harmonics) as input power is being swept. Insert a new rectangular plot and select **vout** to be added. Select **"Fundamental tone in dBm over all sweep values"** to see an output power vs. input power curve as shown in the following snapshot. Insert a marker at pin of 32 dBm to see the output power matching to our optimization.

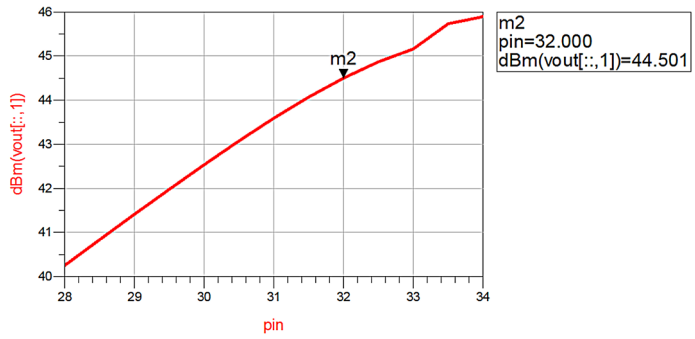


Figure 304.

6. Insert a new rectangular plot and insert PAE to be plotted as shown in the next snapshot.

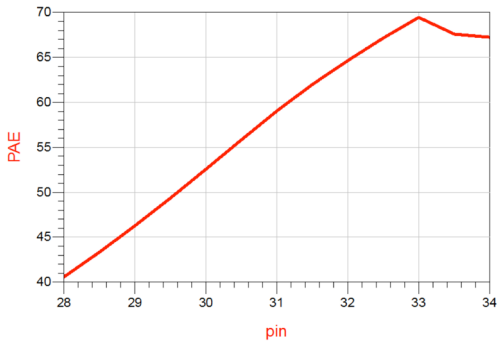


Figure 305.

Step 7: 2-Tone Simulation of Power Amplifier

2-Tone simulations of amplifiers are the recommended method of analysis to find the IMD performance of the designed amplifier. This also provides a clear indication of ACPR (Adjacent Channel Power Ratio) in the case of modulated signals. (Some designers dispute this claim.)

1. From the ADS main window, right click on **"Step5_PA_with_OptimizedMatch"** and select **Copy Cell**.
2. In the Copy Files window, select **Include Hierarchy** and change the suffix from _v1 (or _v2) to "2tone" for all the designs as shown here:

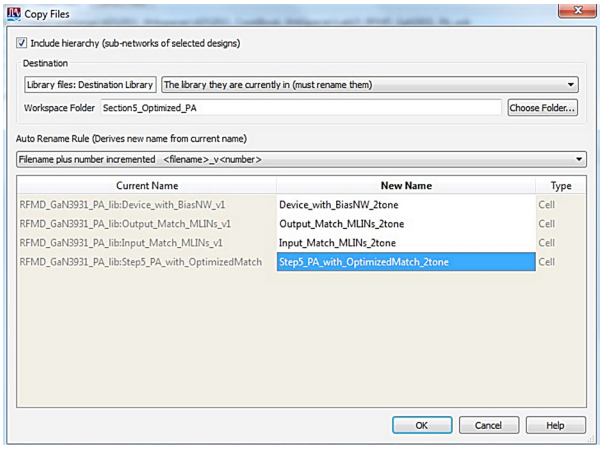


Figure 306.

3. Click **OK** and double click on **"Step5_PA_with_Optimized-Match_2Tone"** to open the schematic.
4. Replace the P_1Tone source with a P_nTone source from the Sources-Freq Domain library.
5. Define two frequencies of **0.9995 GHz and 1.0005 GHz** and power as **polar(dbmtow(pin),0)**.

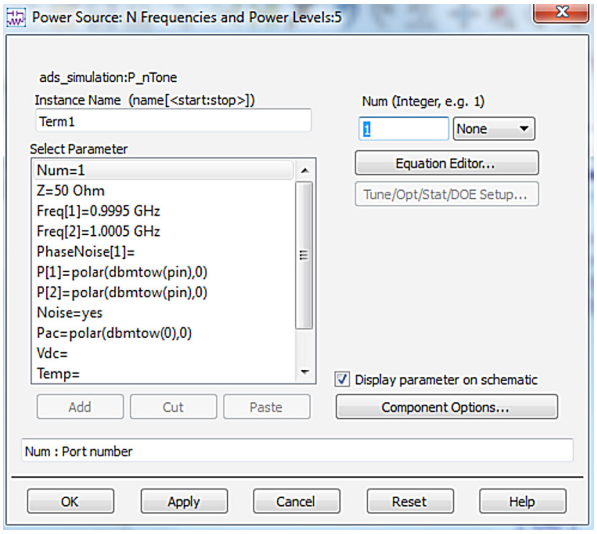


Figure 307.

6. Click **OK**, then double click on the HB controller and specify the following:
   a. Define these two frequencies as analysis frequencies.
   b. Change the Maximum mixing order to see intermodulation products up to the 7th order.
   c. Under the **Sweep** tab, set pin sweep start = 24, stop=32, step-size=1

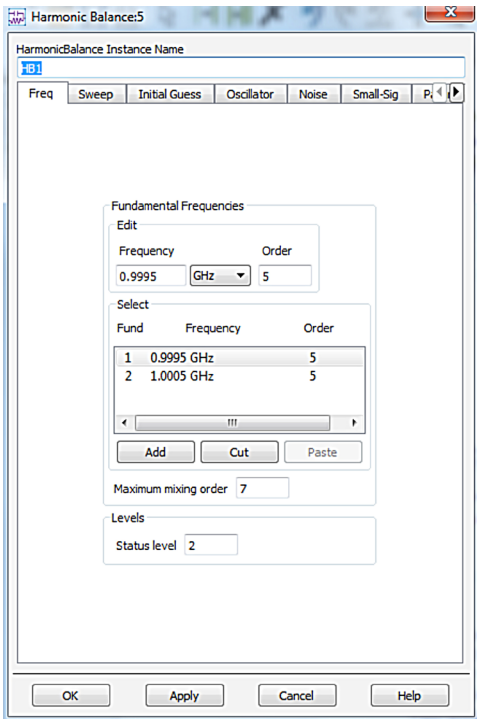


Figure 308.

7. Delete the PAE equation as we will not need it during the 2-Tone simulations.
8. Click on the **Simulate** icon to start the simulation. On the data display, do the following:
   a. Go to **Insert->Slider** and click on the data display. Select **"pin"** and click on **>>Add>>** to see a slider plot as shown below:

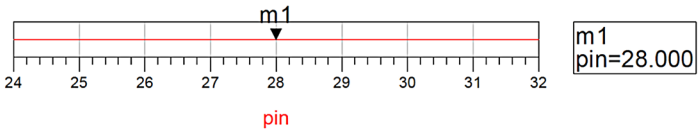


Figure 309.

   b. Insert a new rectangular graph, then select **vout** to be plotted. Select the fundamental tone in dBm over all sweep values from the available plotting options.

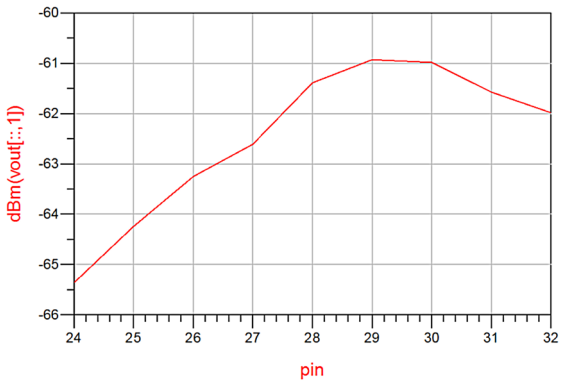


Figure 310..

   c. Click on the **Y-axis label** (that shows dBm(vout[::,1]) and remove the square brackets and its contents so that the Y-axis label displays only **dBm(vout)**. Zoom into frequencies closer to 1 GHz using the Graph zoom icon 
   d. The resulting graph should be similar to the one shown below.

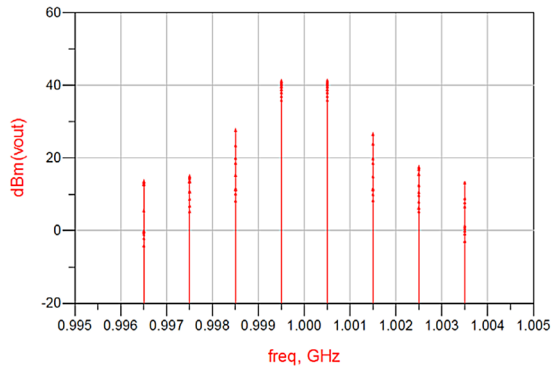


Figure 311.

   e. Click on the Y-axis label and change **dBm(vout) to dBm(vout[m1_pin_index,::])**.This allows designers to vary the slider and observe how the 2-tone results vary accordingly...**try it**!

   f. With the pin value set at 26 dBm (6 dB below our 1-Tone input power), place two markers: one at the main tone on the right side and one on the 3rd order product as shown below.

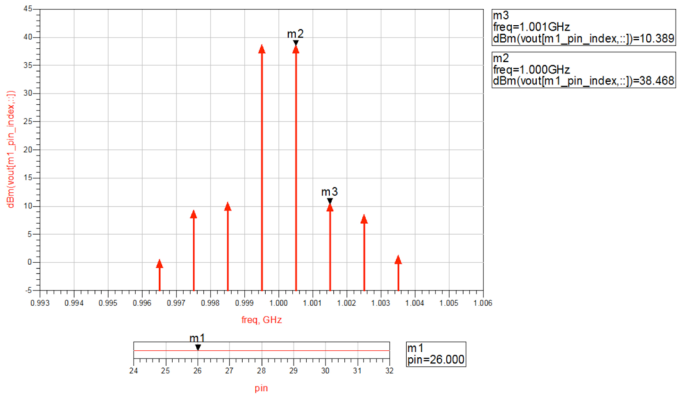


Figure 312.

9. Insert the following two equations on the data display page to calculate PEP (Peak Envelope Power). Insert a table to plot PEP_Watts from the Equations as shown below.

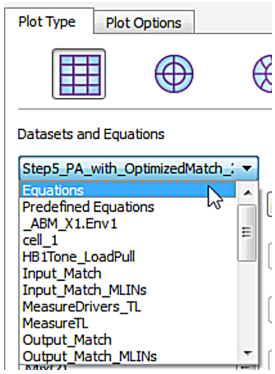


Figure 313.

Eqn P_Watts=dbmtow(m2)

Eqn PEP_Watts=4*P_Watts

freq	PEP_Watts
1.000 GHz	28.110

Figure 314.

Please note that m2 in the dbmtow() equation is the marker name on the main frequency content. Change it to your marker name in the data display.

Step 8: Modulated Signal Analysis of PA (Optional Step)

This step requires familiarity with the Keysight Ptolemy simulator; interested designers can read Chapters 17 and 18 of this book to learn more.

1. Right click on **"Step5_PA_with_OptimizedMatch"** and click on **Copy Cell**. Provide a new name as Optimized_PA and click **OK**.

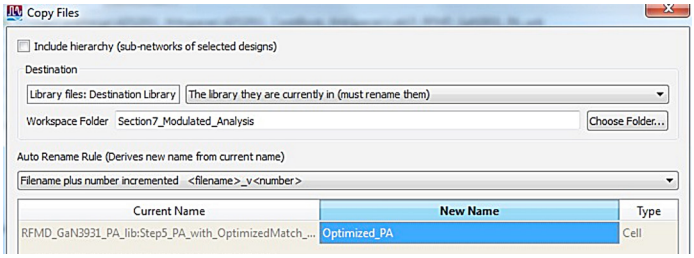


Figure 315.

2. Delete the simulation controller, source, termination, pin variable, etc. so that the schematic looks as below.

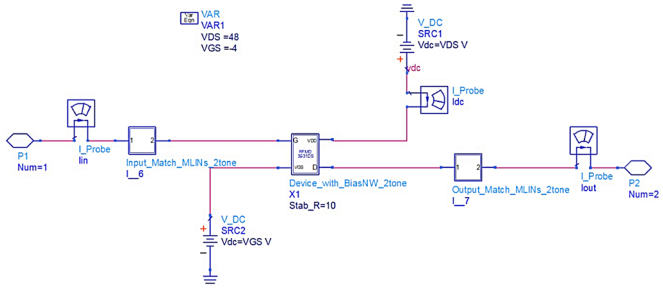


Figure 316.

3. Open a new schematic cell with a name "QPSK_Modulator" and create a Ptolemy design for a QPSK modulator following the method provided in Chapter 18. However, here we shall use **Bit_rate=100MHz** as opposed to the one used in Chapter 18.
4. The QPSK source schematic will look similar to the one shown below.

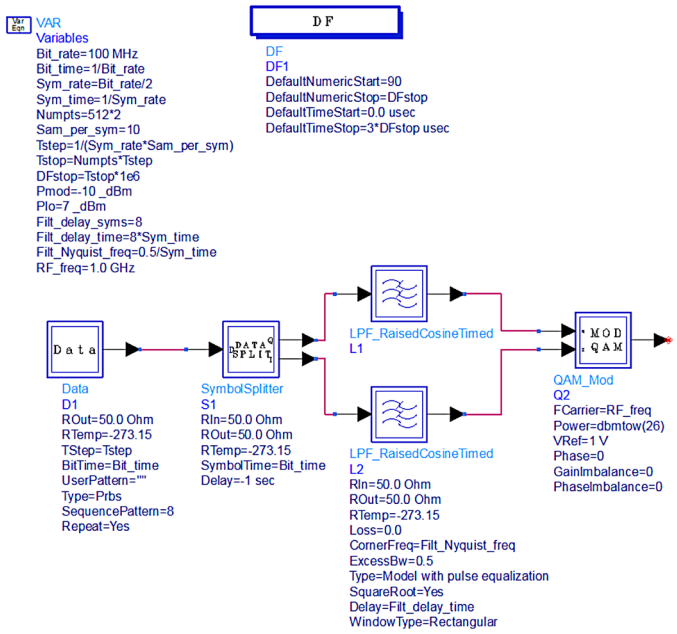


Figure 317.

5. Drag and drop the "Optimized_PA" design as a subcircuit on this QPSK Modulator schematic as shown below. Modulator Power is kept at 26 dBm.
6. Note that Spectrum Analyzer sinks (available in the Sinks library) are named as BeforeAmp and AfterAmp so that we can recognize the modulated spectra in the data display.
7. Place the EnvOutSelector components after our PA subcircuit from the Circuit Cosimulation library (this is a needed component for DSP & RF cosimulation as explained in Chapter 19 of this book).

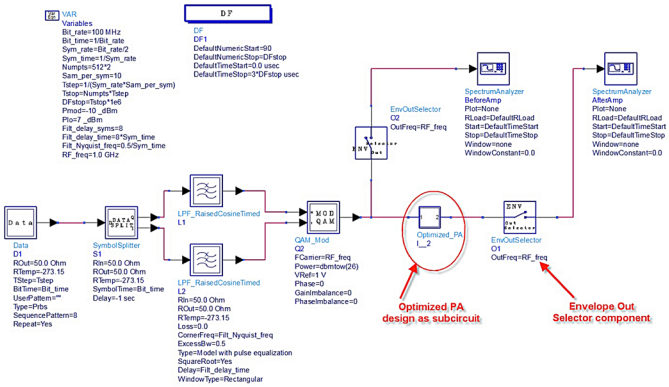


Figure 318.

8. Push into the **Optimized_PA** sub-circuit and place an Envelope simulation controller from the **Simulation-Envelope** library. Set the following in the Envelope Controller:
   a. The default frequency is 1 GHz, matching our requirement so we can leave it as is. Define Time Step = Tstep and Time Stop=Tstop as these are variables defined in the Ptolemy design. Make sure syntax is taken care of.
   b. From the **Fast Cosim** tab, select "**Enable Fast Cosim**."
   c. From **Set Characterization Parameters**, enter Max Input Power (dBm) = 38.

Setting (b) and (c) allows a very fast cosimulation of circuit level designs along with DSP networks.

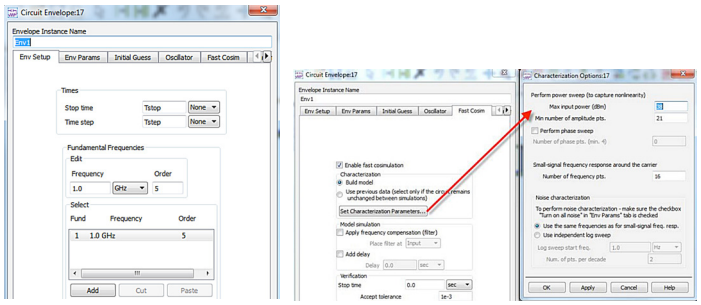


Figure 319.

9. Return to the Ptolemy schematic and run the simulation. Plot two rectangular graphs in the data display: one for the BeforeAmp and one for the AfterAmp modulated spectra.

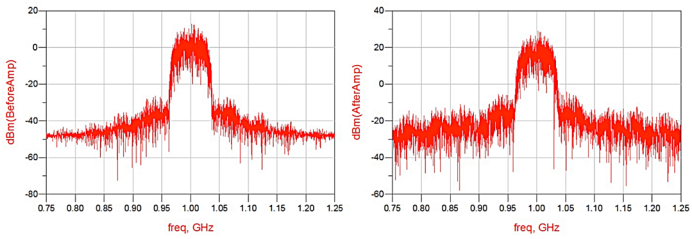


Figure 320..

10. Insert two equations on the data display page to compute the integrated spectrum powers:

```
Eqn PA_IP_Power=spec_power(dBm(BeforeAmp),0.95GHz,1.05GHz)
Eqn PA_OP_Power=spec_power(dBm(AfterAmp),0.95GHz,1.05GHz)
```

Figure 321..

Please note: 0.95 GHz and 1.05 GHz are the band edges as per our bandwidth requirements.

11. Insert a Table, then, from the Equations dataset, select **PA_IP_Power** and **PA_OP_Power** as shown below.

PA_IP_Power	PA_OP_Power
27.893	43.937

Figure 322.

ACPR Calculation:

ACPR is a key metric for wireless modulated signals. It indicates the power leaking into the adjacent band of the operating PA.

Insert four more equations in the data display as shown below. The first two equations compute power in the lower and upper adjacent bands of the amplifier, while the next two equations compute ACPR in these sidebands.

```
Eqn Adj_Ch_Lower=spec_power(dBm(AfterAmp),0.85GHz,0.95GHz)
Eqn Adj_Ch_Upper=spec_power(dBm(AfterAmp),1.05GHz,1.15GHz)
Eqn ACPR_Lower=PA_OP_Power-Adj_Ch_Lower
Eqn ACPR_Upper=PA_OP_Power-Adj_Ch_Upper
```

Figure 323.

Plot the ACPR lower and upper sidebands in the table inserted earlier. It should look similar to the table shown below.

PA_IP_Power	PA_OP_Power	ACPR_Lower	ACPR_Upper
27.893	43.937	33.614	33.516

Figure 324.

Using 89600B With ADS: (Optional)

If designers have a license of VSA software (89600A or 89600B) from Keysight, then it can be used as an interactive sink along with ADS Ptolemy (run ADS in 32-bit mode). The snapshot below shows the power amplifier output with the QPSK demodulator switched on. Note that RMS EVM (Error Vector Magnitude) is 1.5% and ACPR is calculated as 34 dBc, matching to our calculation in the ADS data display.

Figure 325.

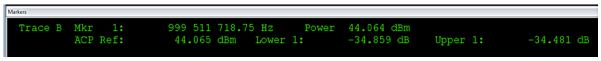


Figure 326.

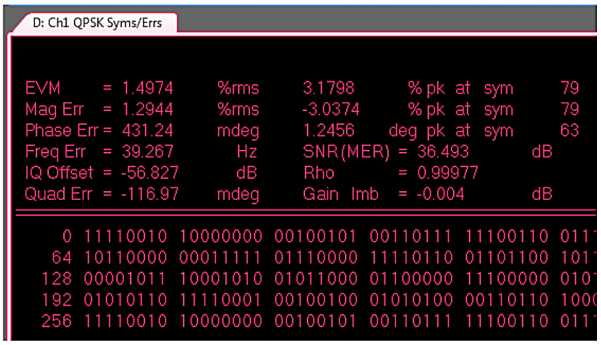


Figure 327.

Design of RF MEMS Switches

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ADS Licenses Used:

1. *Linear Simulation*
2. *Momentum EM Simulator*
3. *Layout*

Theory:

An RF switch is a two-port network that is used for making or breaking an RF circuit. The traditional RF switches-based solid state devices, like diodes and transistors, are limited in performance because of low power handling capability, high resistive losses, etc. MEMS switches have recently become more popular because of better isolation, low losses and capability to operate at very high frequencies but with limited power handling capability and reduced dc voltage.

RF MEMS switches are composed of a thin membrane that can be electro-statically actuated to the RF path using a DC bias voltage. There are two basic switches that are used in RF circuit design: the shunt switch and the series switch. The ideal series switch results in an open circuit in the transmission line when no bias voltage is applied (Up state position) and it results in a short circuit in the transmission line when the bias voltage is applied (Down state position). The shunt switch is placed in shunt between the transmission line and the ground. Depending on the applied bias voltage, it either leaves the transmission line undisturbed or connects it to ground. Therefore, the ideal shunt switch results in zero insertion loss when no bias is applied (Up state position) and infinite isolation when bias is applied (Down state position) as shown in Figure 328.

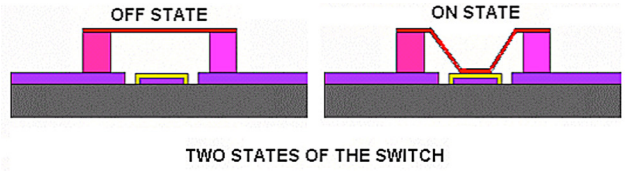


Figure 328. Geometry of the RF MEMS Shunt Switch in ON and OFF State.

A shunt capacitive MEMS switch consists of a thin metallic membrane bridge suspended over the center conductor of a coplanar waveguide or microstrip line and fixed at both ends to the ground conductors of the CPW line. Thus, the tunable capacitor can be associated with the movable electrode suspended on the top of a fixed electrode. The suspended electrode is movable in the vertical direction normal to the substrate. The gap between the movable and the fixed electrodes can be adjusted electro-statically by applying a tuning voltage resulting in a change in its capacitance. The electrostatic actuation is normally preferred over other actuation mechanisms because of its low power consumption.

When an electric field is applied to a parallel plate system, the movable plate starts moving towards the fixed plate as the result of the electrostatic force. This force is distributed along the length of the movable plate and, when the threshold bias voltage is reached, the plate snaps down to the bottom plate and the applied voltage no longer controls the beam. The equilibrium between the electrostatic attracting force and the force at the supports holds only for a deflection smaller than one-third of the initial gap between them.

RF MEMS switches are extensively used for high performance switching applications at microwave and millimeter wave frequencies. They are used along with conventional components like filters, antennas, etc. to bring about frequency tuning. RF MEMS shunt switches are also used for the design of high performance Phase Shifters.

Objective:

To design a MEMS shunt switch at 4 GHz and simulate the performance using ADS.

Design of MEMS Shunt Switch

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the RF MEMS switch.
2. Synthesize the physical parameters (length & width) for the $\lambda/4$ CPW lines with an impedance of Z_0. (Z_0 is the characteristic impedance of CPW line = 50Ω)
3. Determine the material (type of movable membrane, spring constant etc.) and physical parameters of the switch (length & width) so as to satisfy the given requirements of pull down voltage given by

$$V_p = \sqrt{\frac{8k}{27\varepsilon_o W w}\, g_o^3} \quad V.$$

Where,

W is the width of the CPW center conductor

w is the width of the MEMS membrane

k is the spring constant of the MEMS membrane

g_0 is the initial gap between the CPW center conductor and the MEMS membrane

Layout Simulation Using ADS:

1. Calculate the physical parameters of the transmission line from the electrical parameters like Z_0, Frequency and electrical length of λ/4 CPW line. The physical parameters can be synthesized using LineCalc in ADS as shown in Figure 329 for the following parameters.

   Frequency : 4 GHz

   Substrate Thickness : 675 microns

   Dielectric Constant : 11.7

   Characteristic Impedance : 50 Ω

   Electrical Length : 90^0

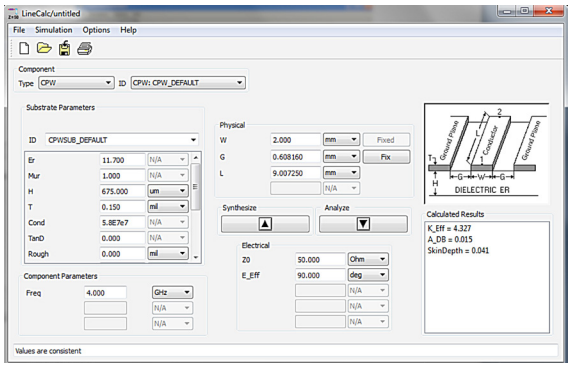


Figure 329. LineCalc window of ADS showing the synthesis of physical parameters of the λ/4 CPW transmission line.

2. The Physical parameters of the λ/4 CPW line for the 50Ω (Z_0) line for the frequency of 4 GHz as synthesized from LineCalc is given as follows.

   50Ω Line:

   Width = 2 mm
   Length = 9 mm
   Gap = 0.608mm

3. Calculate the physical parameters of the MEMS switch as given in design step 3. For example, chose the physical parameters of the MEMS Switch as follows so as to have a pull down voltage of 10 V.

   Length = 4 mm
   Width = 0.25 mm
   Thickness = 2 microns
   Initial gap = 15 microns

4. Create a model of the λ/4 CPW transmission line in the layout window of ADS. The Model can be created as follows. Click **Insert>>rectangle** and the cursor appears on the screen with dotted lines. Now click **Insert >>Coordinate Entry** and give the coordinates for the rectangle as shown in Figure 330. For example, to create a rectangle of length and width 2 mm and 9 mm we may enter the coordinates as (0, 0) and (2, 9).

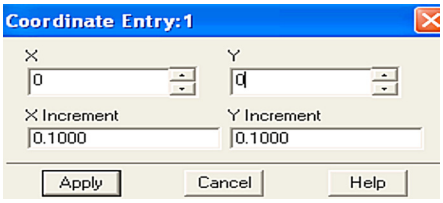


Figure 330. Figure showing the coordinate entry dialog box.

5. Alternatively, we can use the 3 coupled line model from **TLines-Multilayer** library and select ML3CTL_V, which will allow widths of the transmission line to be different. Enter parameters as below

   Length = 9 mm

   W[1] = 4 mm (ground width)

   S[1] = 0.6 mm (spacing between conductor and ground)

   W[2] = 2 mm (main line width)

   S[2] = 0.6 mm (spacing between conductor and ground)

   W[3] = 4 mm (ground width)

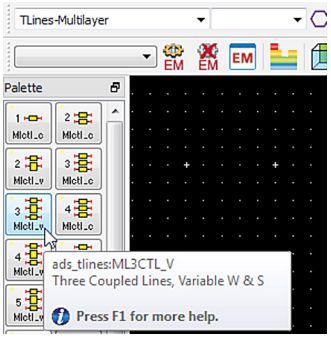


Figure 331.

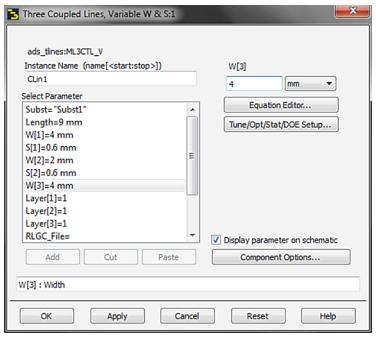


Figure 332.

6. Once done, layout will look as shown below.

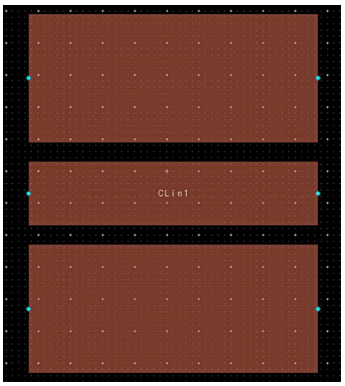


Figure 333. Model of the CPW line in the layout window of ADS.

7. Assign Pins for the CPW transmission line by clicking the Pin icon and pasting them in the circuit. The Pins have to be assigned both on the center conductor and the ground plane of the CPW line. For easy remembrance, place Pin 1 and 2 on the main line and then P3 & P4 on each side of P1 and P5 & P6 on each side of P2, this will help us while doing the Port assignment during the EM simulation setup.

8. Draw the next layer representing the post of the MEMS switch. To do this, select the **hole** as the Entry layer from the drawing layer drop down box as shown in the Figure 334 below.

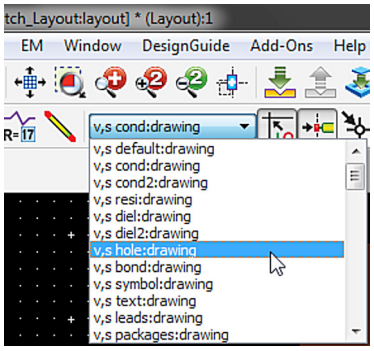


Figure 334. Selection of hole layer using the dropdown box.

9. Draw the posts with a dimension of width 0.15 and length 0.25 on the ground layers on each side of the center conductor as shown in Figure 335. These posts will provide the support the MEMS membrane in the switch. The posts should be placed in such a way that they lie in the two corners of the MEMS membrane that we will draw later.

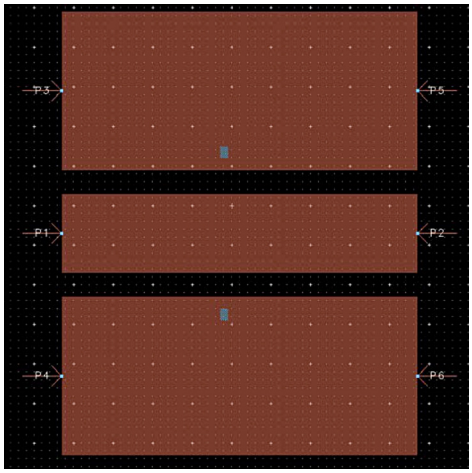


Figure 335.. Layout of the CPW line with the posts drawn using the resi layer.

10. Draw the MEMS membrane layer by selecting the cond2 layer as in earlier step. The membrane is drawn above the post layer as shown in Figure 336 below.

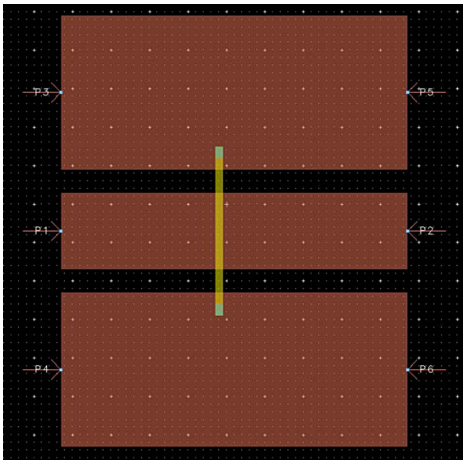


Figure 336. Layout of the RF-MEMS Shunt Switch.

11. Click on the Substrate Editor icon and select 25 mil Alumina template . From the template of the default substrate, right click and select Insert Substrate Layer Below and repeat the same action to Insert Substrate Layer Above.

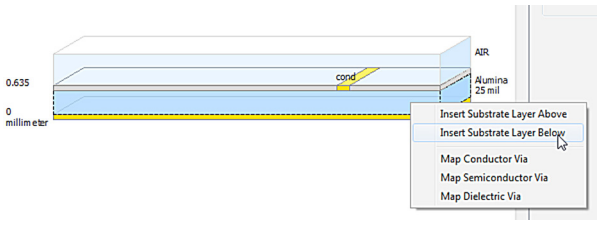


Figure 337..

12. Change these 2 new substrate types to AIR (default definition available). Once done we shall have the following type of dielectric stack-up.

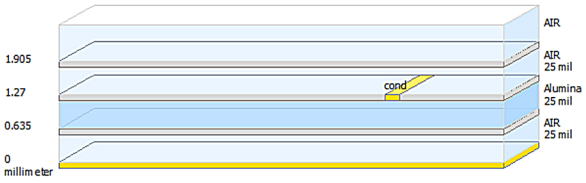


Figure 338..

13. From this substrate, do the following actions to prepare the substrate for a MEMS simulation:
    a. Change the AIR layer above cond to have thickness of 15 um to represent the Up state of the switch
    b. Right-click on the top of the 15um AIR layer junction and select Map Conductor layer and make sure it is cond2, which is the same layer we have used to draw the switch membrane in our layout

c. Add a new Silicon dielectric with Er=11.7 as described in the EM simulation chapter and set the height as 675um
d. Right-click on the Silicon substrate and select Map Conductor via and make sure the layer name is “hole,” which is the same as we have used to draw the post in layout
e. Right-click on the bottom most Cover and select Delete Cover so that there is no ground at the bottom.

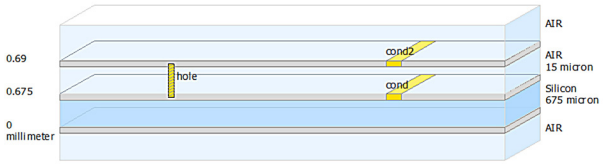


Figure 339.

14. Open the EM Setup window and go to the Ports option, select Port 3-6 right-click and select “delete” so that these get removed from the Port list as shown below

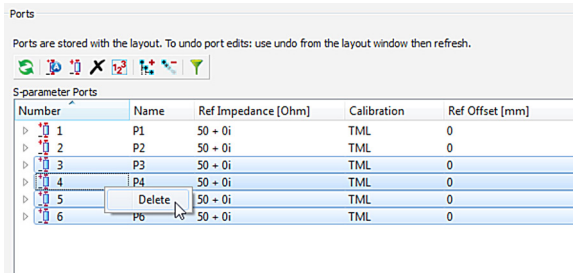


Figure 340.

15. Expand Port 1 and drag and drop P3 and P4 one by one on –Gnd terminal so that they are used as ground ports for Port1. Do the same thing for P5 and P6 and attach it to –Gnd of Port2. Once done, it should be configured as shown below

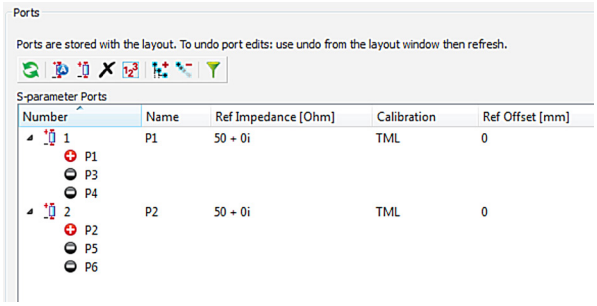


Figure 341.

16. Go to **Options->Mesh** tab and switch on the Edge Mesh and set Cells/Wavelength=50.

17. Change the Simulation Mode to Momentum RF for faster simulation as the structure is smaller. Click on the simulate button and plot the required response in the data display window to see the switch performance in the Up state.

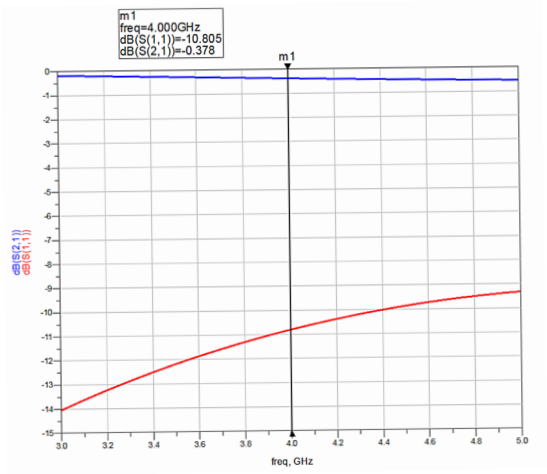


Figure 342.

Switch Simulations in the Down State:

1. To simulate switch performance in the Down state, we need to change the thickness of AIR layer to something like 0.1 um between cond and cond2 layers to represent the membrane movement due to applied voltage.
2. Open the substrate editor and go to **File->Save As** and save the substrate with new name e.g. Switch Down State as shown below

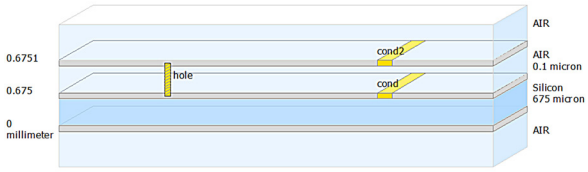


Figure 343.

3. Go to the EM setup window and change the substrate to Switch State Down as shown below

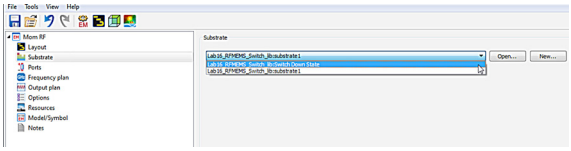


Figure 344.

4. From Output Plan, select “This text” and enter some name by which we shall recognize this new simulation dataset so that the older dataset is not overwritten, as shown below

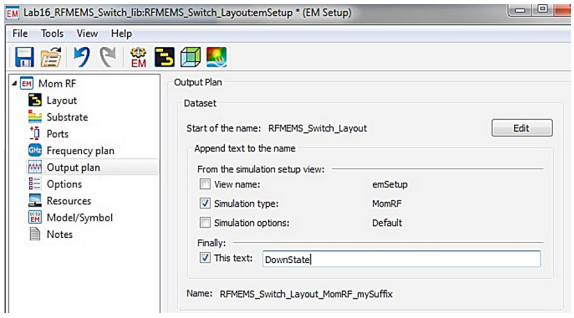


Figure 345.

5. Click on the Simulate button and plot the required response to see the switch's performance in the Down state as shown below.

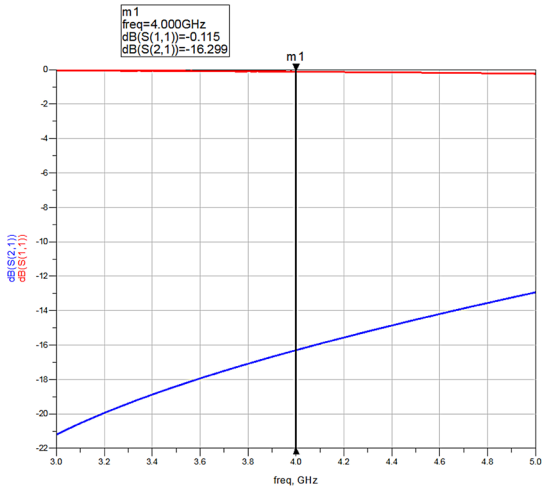


Figure 346.

Results and Discussions:

From the results, the RF MEMS switch has an insertion loss (S_{21}) of -0.3 dB and return loss (S_{11}) of < -10 dB in the Down state and the switch has an insertion loss (S_{21}) of -16 dB and return loss (S_{11}) of about -0.1 dB in the up state thus exhibiting decent switch characteristics, this performance can be further optimized if necessary.

Circuit Model of the MEMS Shunt Switch

Theory

The MEMS switch is modeled by two short sections of transmission lines and a lumped CLR model of the bridge with the capacitance having the Up state/Down state values. The transmission line is of length (w/2) + l where l is the distance from the reference to the edge of the MEMS bridge. Typical values of the inductance are 7 to 8 pH and series resistance are .2 to .3 ohms.

The shunt impedance of the switch is given by

$$Z_s = R_s + j\omega L + 1/j\omega C$$

With C = C_u or C_d depending on the position of the switch.

The LC series resonant frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The impedance of the shunt switch can be approximated by

$$Z_s = \begin{cases} 1/j\omega C & \text{for } f << f_0 \\ R_s & \text{for } f = f_0 \\ j\omega L & \text{for } f >> f_0 \end{cases}$$

The CLR model behaves as a capacitor below the LC series resonant frequency and as an inductor above this frequency. At resonance the CLR model reduces to the series resistance of the MEMS bridge. The cutoff frequency is defined as the frequency where the ratio of the off and on impedance degrades to unity and is

$$F_c = 1/2\pi C_u R_s$$

Typical Design:

The Values of Capacitance is given by the formula

$$C = \varepsilon W w/g$$

Where W is the width of the center Conductor of CPW = 2 mm

w is the width of the switch membrane = 0.25mm

g is the gap between the center conductor and MEMS membrane

Up state:

The Gap g = 15 microns

Thus C_{up} = 0.29 pF

Down state:

The Gap g = 15 microns

Thus C_{down} = 44 pF

Schematic Simulation Using ADS

1. Open the Schematic window of ADS
2. From the TLines – Waveguide library select two CPW lines and place them on the schematic window. Double click on the transmission lines and give the physical parameters as follows

   Width = 2 mm

   Length = 4.5 mm

   Gap = 0.608mm

3. From the lumped components library select the appropriate components necessary for the equivalent circuit of the MEMS switch. Click on the necessary components and place them on the schematic window of ADS.

Create the circuit model of the MEMS switch on the schematic window with  appropriate lumped components and complete the circuit with wires.

UP State

4. Double click on the lumped components values and enter their values. The values are calculated from the upstate and down state capacitances of the switch as given in design procedure. The values of resistance and inductance are the typical values obtained for a MEMS switch.

   Capacitance C = 0.29 pF
   Resistance R = 1 Ω
   Inductance L = 1 pH

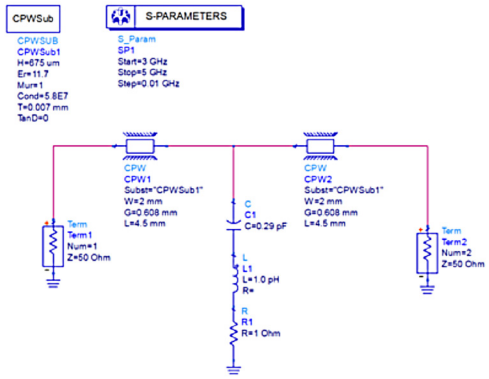


Figure 347.

5. Click on the Simulate icon and plot the required response in data display to observe the switch characteristics in Up state

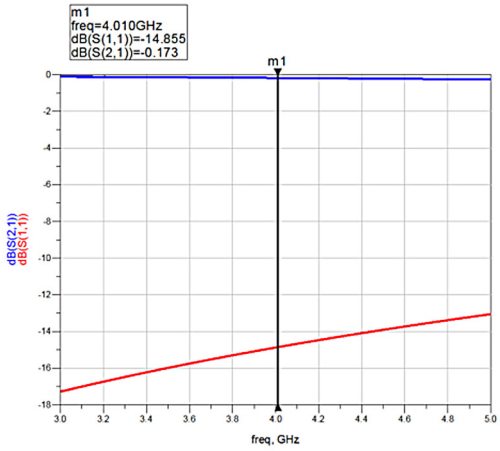


Figure 348.

Down State

6. Double-click on the lumped components values and enter their values.

   Capacitance C = 44 pF
   Resistance R = 1 Ω
   Inductance I = 1 pH

7. Simulate the circuit to view the scattering parameters of the switch in Down state. The results of the simulation are shown in the next figure.

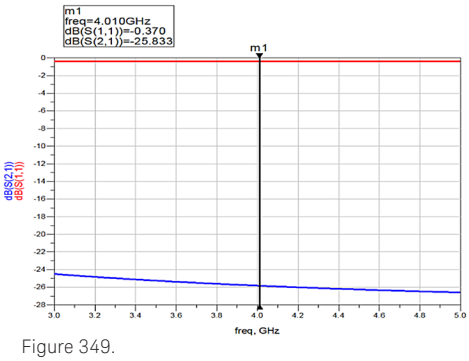


Figure 349.

Results and Discussions:

From the results, the MEMS switch circuit has an insertion loss (S_{21}) of -0.17 dB and return loss (S_{11}) of about -15 dB in the Down state. The switch has an insertion loss (S_{21}) of -25 dB and return loss (S_{11}) of about -0.3 dB in the Up state, thus exhibiting good switch characteristics.

Getting Started with ADS PTolemy

ADS Licenses Used:

- *ADS PTolemy Simulator*

The ADS Ptolemy software provides the simulation tools you need to evaluate and design modern communication systems products. Today's designs call for implementing DSP algorithms in an increasing number of portions of the total communications system path, from baseband processing to adaptive equalizers and phase-locked loops in the RF chain. Co-simulation with ADS RF and analog simulators can be performed from the same schematic.

Using the ADS Ptolemy simulator you can:

- Find the best design topology using state-of-the-art technology with more than 500 behavioral DSP and communication systems models
- Co-simulate with RF and analog simulators
- Integrate intellectual property from previous designs
- Reduce the time-to-market for your products

ADS Ptolemy features:

- Timed synchronous dataflow simulation
- Easy-to-use interface for adding and sharing custom models
- Interface to test instruments
- Data display with post-processing capability

Theory of Operation for ADS Ptolemy Simulation

- ADS Ptolemy provides signal processing simulation for ADS's specialized design environments. Each of these design environments captures a model of computation, called a domain, which has been optimized to simulate a subset of the communication signal path. ADS domains that are part of ADS Ptolemy, or can co-simulate with ADS Ptolemy are:

Domain	Simulation technology	Controller	Application area
Synchronous data flow (SDF)	Numeric data flow	Data flow	Synchronous multi-rate signal processing simulation
Timed Synchronous Dataflow (TSDF)	Timed data flow	Data flow	Baseband and RF functional simulation \ (e.g., antenna and propagation models, timed sources)
Circuit envelope	Time- and frequency-domain analog	Envelope	Complex RF simulation
Transient	Time-domain analog	Transient	Baseband analog simulation

- In ADS Ptolemy, a complex system is specified as a hierarchical composition (nested tree structure) of simpler circuits. Each sub-network is modeled by a domain. A sub-network can internally use a different domain than that of its parent. In mixing domains, the key is to ensure that at the interface, the child sub-network obeys the semantics of the parent domain.
- Thus, the key concept in ADS Ptolemy is to mix models of computation, implementation languages, and design styles, rather than trying to develop one, all-encompassing technique. The rationale is that specialized design techniques are more useful to the system-level designer, and more amenable to a high-quality, high-level synthesis of hardware and software.

Synchronous Dataflow

Synchronous dataflow (SDF) is a special case of the dataflow model of computation. The specialization of the model of computation is to use dataflow graphs where the flow of control is completely predictable at compile time. It is a good match for synchronous signal processing systems, those with sample rates that are rational multiples of one another.

The SDF domain is suitable for fixed and adaptive digital filtering, in the time- or frequency-domains. It naturally supports multi-rate applications, and its rich component library includes polyphase FIR filters. The ADS examples directories contain application examples that rely on SDF semantics. To view these examples, choose **File > Open > Example**; select the *DSP/dsp_demos_wrk* directory for one group of SDF examples.

SDF is a data-driven, statically scheduled domain in ADS Ptolemy. It is a direct implementation of the techniques given by Lee [2] [3]. *Data-driven* means that the availability of data at the inputs of a component enables it; components without any inputs are always enabled. *Statically scheduled* means that the firing order of the components is periodic and determined once during the start-up phase. It is a simulation domain, but the model of computation is the same as that used for bit-true simulation of synthesizable hardware.

Timed Synchronous Dataflow

Timed synchronous dataflow (TSDF) is an extension of SDF. TSDF adds a timed data type. For each token of the timed type, both a time step and a carrier frequency must be resolved.

ADS examples directories contain numerous application examples that rely on TSDF semantics. To view these examples, choose **File > Open > Example**, a dialog box appears. Select the *DSP/Modem-Timed_wrk* directory for one group of TSDF examples.

Note that the ADS Ptolemy (Pt) simulation time-domain signals are different from those used for Circuit Envelope (CE) and Transient (T) simulation.

- For Pt, the simulation time step is not global and the input signals for different components may have a different time step. However, the simulation time step at each node of a design, once set at time=0, remains constant for the duration of the simulation. The time step is initially set by the time domain signal sources or numeric to timed converters. The time step in the data flow graph may be further changed due to upsample (decreases the time step by the upsampling factor) and/or down sample (increases the time step by the downsample factor) components. The time step associated with signals at the inputs of the timed sinks may or may not be the same as the one that was initiated by the timed sources or numeric to timed converters. This is dependent on any up or down sampling that may have occurred in the signal flow graph.
- For CE, the simulation time step is set by the simulation controller and is constant for the duration of the simulation. This is global for all components simulated in the design.
- For T, the simulation maximum time step is set by the simulation controller, but the actual simulation time step may vary for the duration of the simulation. This simulation time step is global for all components simulated in the design.
- For Pt, each timed sink that sends data to Data Display has time values that are specific to the individual sink and may or may not be the same as the time values associated with data from other timed sinks.
- For CE and T, all time-domain data sent to Data Display has the same global time value.
- For CE, a time-domain signal may have more than one carrier frequency associated with it concurrently. The carrier frequencies in the simulation are harmonically related to the frequencies defined in the CE controller and their translated values that result from nonlinear devices.
- For Pt, a time-domain signal has only one characterization frequency associated with it. This characterization frequency is also typically the signal carrier frequency. However, the term carrier frequency is more typically used to mean the RF frequency at which signal information content is centered. A signal has one characterization frequency, but the signal represented may have information content centered at one or more carrier frequencies. This would occur when several RF bandpass signals at different carrier frequencies are combined to form one total composite RF signal containing the full information of the multiple carriers.

Example

Two RF signals and their summation:

Arf = Ai*cos(wa*t) - Aq*sin(wa*t) with carrier frequency wa

Brf = Bi*cos(wb*t) - Bq*sin(wb*t) with carrier frequency wb

The summation of these two signal, Crf, can be represented at one characterization frequency, wc, as follows:

Crf = Ci*cos(wc*t) - Cq*sin(wc*t) with carrier frequency wc

where

wc = max(wa, wb)

Ci = Ai + Bi*cos((wa-wb)*t) + Bq*sin((wa-wb)*t)

(assuming wa > wb)

Cq = Aq - Bi*sin((wa-wb)*t) + Bq*cos((wa-wb)*t)

(assuming wa > wb)

Time Step Resolution

In TSDF, each Timed arc has an associated time step. This time step specifies the time between each sample. Thus, the sampling frequency for the envelope of a Timed arc is 1/time step.

The sampling frequency is propagated over the entire graph, including both Timed and numeric arcs. To calculate a time step, the SDF input and output numbers of tokens consumed/produced are used.

For any given SDF or TSDF component, the sampling frequency of the component is defined as the sampling frequency on any input (or output) divided by the consumption (or production) SDF parameter on that port. After a sampling frequency is derived for a given component, it is propagated to every port by multiplying the component's rate with the SDF parameter of the port. A sample rate inconsistency error message is returned if inconsistent sample rates are derived.

Carrier Frequency Resolution

Each timed arc in a timed dataflow system has an associated carrier frequency (F_c). These F_c values are used when a conversion occurs between timed and other data types, as well as by the timed components.

The F_c has either a numerical value, which is greater than or equal to zero ($F_c \geq 0.0$), or is undefined (F_c = UNDEFINED). All timed ports have an associated $F_c \geq 0.0$. Non-timed ports have an UNDEFINED F_c. During simulation, all F_c values associated with all timed ports are resolved by the simulator. The resolution algorithm begins by propagating the F_c specified by the user in the timed sources parameter *Fcarrier* until all ports have their associated F_c. At times, the user may have specified incompatible carrier frequencies, and ADS Ptolemy will return an error message.

In the feedforward designs, the algorithm will converge quickly to a unique solution. In the designs with feedback, the algorithm takes additional steps to resolve the carrier frequency at all pins. For feedback paths, a default F_c is assigned by the simulator. This default F_c is then propagated until the F_c converges on the feedback path. This F_c is occasionally non-unique. To specify a unique value, use the SetFc timed component.

Input/Output Resistance

Resistors can be used with timed components. Resistors provide a means to support analog/RF component signal processing. They provide definition of analog/RF input and output resistance, additive resistive Gaussian thermal (Johnson) noise, and power-level definition for time-domain signals.

Though resistors are circuit components, they are used in the data flow graph by defining their inputs from the outputs of connected TSDF components and their outputs at connected TSDF component inputs.

Representation of Data Types

ADS Ptolemy schematics contain component stems with different colors and thicknesses. Each component input and output pin has an associated data type, and each type is represented in the component symbol by use of a color code and a thickness of stem. And each component stem may have single or multiple arrowheads. The following table lists the data types.

Component Stem Color and Thickness

Data type	Stem color	Stem thickness
Scalar fixed point	Magenta	Thin
Scalar floating point (real)	Blue	Thin
Scalar integer	Orange	Thin
Scalar complex	Green	Thin
Matrix fixed point	Magenta	Thick
Matrix floating point (real)	Blue	Thick
Matrix integer	Orange	Thick
Matrix complex	Green	Thick
Timed	Black	Thin
Any type	Red	Thin

How to set Tstep in a TSDF simulation

Tstep is the single most important factor in a TSDF simulation. The Tstep setting will determine the effective analysis BW of the simulation. All signals present within the analysis BW will determine the result in a simulation, including aliased waveforms.

For bandpass signal types, the analysis BW will be equal to 1/Tstep and for baseband signal types the analysis BW will be equal to 1/(2*Tstep). If you think about this from a Nyquist point of view, the Tstep must be set, at a maximum, to ½ of the shortest period signal in the simulation. Since Ptolemy only treats the complex envelope of a signal, the Tstep is always set relative to the BW of the complex envelope and not the carrier frequency. So, thinking in terms of the signal being analyzed, Tstep=1/(EnvBW) for bandpass signals and Tstep=2/(BBBW) for baseband signals, where EnvBW is the BW of the complex envelope of the modulated signal being analyzed and BBBW is the BW of the baseband signal being analyzed. As a rule of thumb, many simulations are over sampled beyond to simple Nyquist rate.

Timed Filters
Timed Linear
Timed Modem
Timed Nonlinear
Timed RF Subsystems
Timed Sources

Figure 350.

In both modulated and baseband cases, we are sampling the baseband portion or complex envelope of the waveform and not the carrier. In the modulated case the baseband BW contains real and imaginary signal information, or I and Q, while the non-modulated case typically we are sampling only a real valued signal.

For a more thorough treatment of the TSDF simulation domain and its signal types please refer to the online manual set for ADS. The appropriate information can be found in chapter 9 of the Keysight Ptolemy Simulation manual as well as the Introduction section of the Timed Non-Linear, Timed Linear, and Timed Filter sections of Signal Processing Components manual.

Signal Conversions: How to Go From SDF to TSDF and Vice-Versa

The interface between SDF and TSDF is analogous to the interface formed by DACs and ADCs in a real system. Everything between the DAC and ADC in a transceiver (with the DAC being in the TX path while the ADC is in the RX path) is analog/RF while everything before the DAC and everything after the ADC is typically digital, representing discrete signal processing. So, considering a typical simulation of a complete transceiver in Ptolemy, the purely digital and algorithmic portions of the design will be treated in SDF while the analog/RF portions will be in TSDF.

There are many ways to convert timed waveforms into SDF (or numeric) waveforms and vice versa. In the case of bandpass (or modulated) signals, conversion has to take place in such a way as to keep the complex nature of the signal intact. The following components depict typical waveform conversions for going from Timed to Numeric and then Numeric to Timed:

ADS PTolemy Component Libraries:

Key component libraries of ADS Ptolemy are

1. Numeric

Numeric libraries provides all the necessary blocks for performing SDF simulations i.e. classic DSP mode of operation in ADS. There are various categories as shown in the snapshot here, which are mostly self-explanatory.

Numeric Advanced Comm
Numeric Communications
Numeric Control
Numeric Fixed-Point DSP
Numeric Logic
Numeric Math
Numeric Matlab
Numeric Matrix
Numeric Signal Processing
Numeric Sources
Numeric Special Functions

Figure 351.

2. Timed

Timed library blocks enable designers to perform simulations based on TSDF i.e. RF or RF envelope simulations for Mixed Signal System simulations.

3. Signal Converters

Signal Converter libraries provides the necessary blocks to perform Data type convertors e.g. Float to Timed, Rect to Complex etc.

4. Sinks

Sinks library provides variety of data collection sinks such as Timed, Spectrum Analyzer, EVM, BER etc.

5. Interactive Controls and Displays

ADS provide real-time interactive controls and display options that can be used by designers to plot data on-the-go. These displays are based on TCL (Terminal Control Language) scripting.

6. Instruments

The instruments library provides source and sink components for various Keysight instruments such as Vector Signal Generators, Logic Analyzers, Scopes, VSA etc. Using these links we can transfer the data from ADS to Instruments & vice-versa through ADS Connection Manager Server software.

Lab1: Getting Started With Numeric (DSP / SDF) Simulations

The objective of this first lab is to understand some of the basic use-models of ADS PTolemy and understand the concept to using Sink, Interactive Control and Displays etc.

1. Create a new workspace from **File->New->Workspace** and make sure the DSP library is selected in the library selection window as shown below

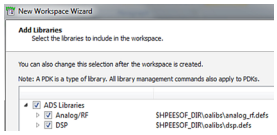


Figure 352.

2. Open a new schematic cell and place the following components from the library
   a. SineGen source from Numeric Sources library (note the blue color stem, which indicates that the output from SineGen would be of Float data type)
   b. Numeric Sink from Sinks library
   c. DF (Data Flow / PTolemy) controller from the Common Components library. Note that the DF controller has Numeric Start, Stop & Time Start, Stop that will be used as per the blocks in the design. Currently, there is no Timed block in our design, hence Time start & stop will be ignored.

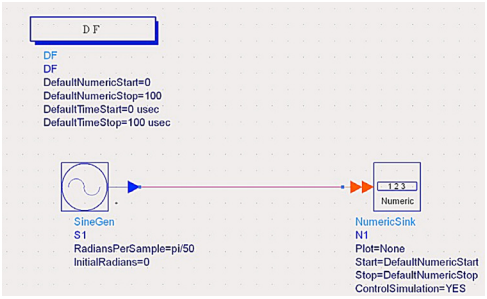


Figure 353.

3. Simulate the design by pressing F7 or Simulate icon
4. Insert a rectangular graph in the data display window and select N1 (name of the numeric sink, designers can rename the sink as needed) data to plot to observe the data as shown below. Please note that Y-axis limits can be changed to +1.5 to -1.5 as shown below.
5. Insert a TkPlot from the Interactive Control and Displays library and connect it to the SineGen source as shown below. TkPlot is used to see the data on a real-time basis, which is very useful before running a long simulation to make sure the design is providing the expected results. Change the yRange on TkPlot to -1.5 1.5 to scale the Y-axis of the display window.

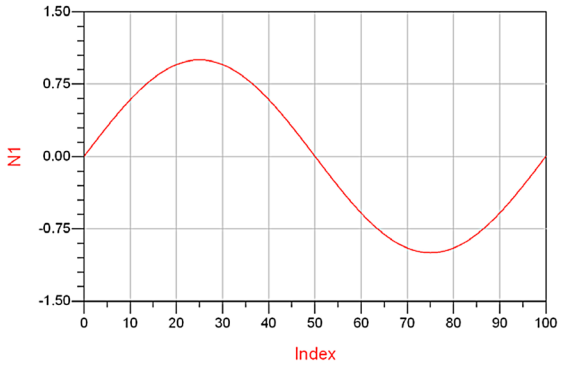


Figure 354. Notice the X-axis on the graph in named "Index" (which is the data sample index as per the RadiansPerSample setting in SineGen source)

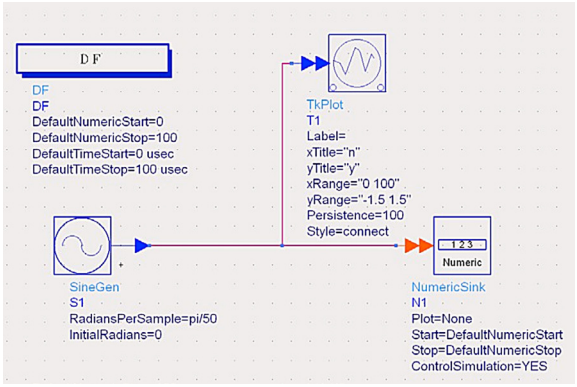


Figure 355.

6. Click the Simulate icon and observe the TkPlot, which will run in continuous mode till we click on the Quit button as shown below. Once we click on Quit, the normal data display with the N1 result will appear.

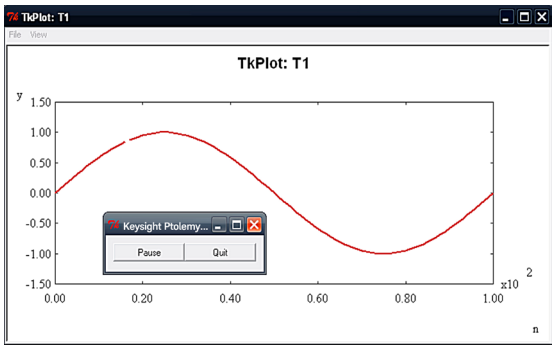


Figure 356. Please note TkPlots are qualitative plots and not quantitative, hence we can't place markers, etc. for readout.

7. Now let us understand how signal / domain conversion can be performed to form a very basic mixed mode simulation. Place the following components in the design:

   a. Insert Timed sink and Spectrum Analyzer sink from Sinks library
   b. Insert Float to Timed converter from Signal converter library.

Modify the following in the design:

a. Delete or Deactivate Tk Plot
b. Define TStep=1nsec in Float to Timed converter
c. Change the DefaultTimeStop=100nsec in the DF controller

Once completed, the schematic should look as below:

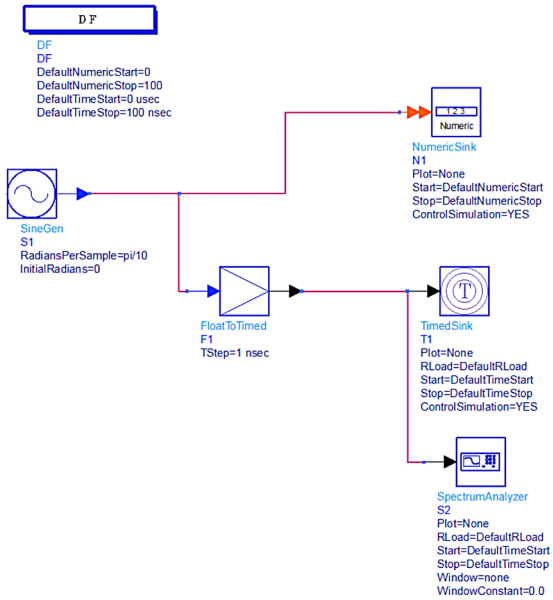


Figure 357.

8. Simulate and add a new rectangular plot along with previously plotted N1 (Numeric sink) and select T1 (Timed Sink) and notice the time domain waveform with X-axis is denoted as time.

Add a new rectangular graph and plot S2 (Spectrum Analyzer) in dBm to see the 1-tone spectrum waveform.

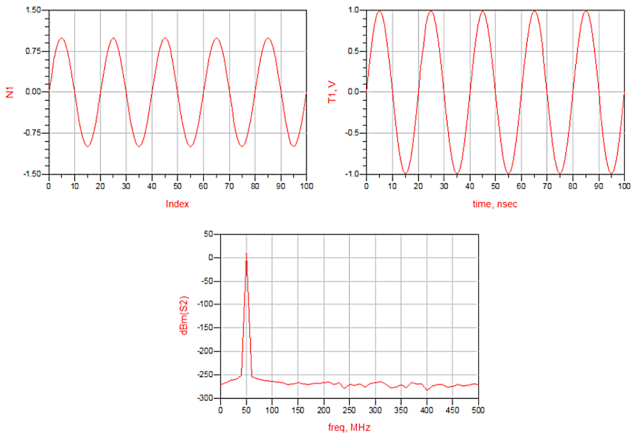


Figure 358.

Notice that the resolution of the spectrum plot is not good. This is due to only having a 100 sample point resolution i.e. 100 nsec (Stop Time) /1 nsec (Sampling Time) = 100.

Increase the DefaultTimeStop = 1024 nsec and observe the data display again. Now the Spectrum plot should have better resolution. *The more samples you have, the better will be the spectrum resolution.*

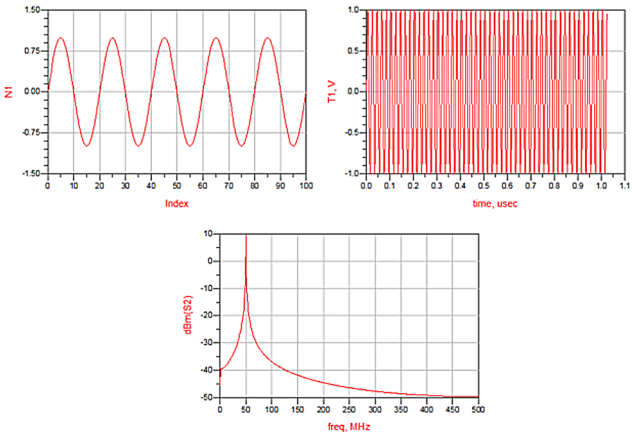


Figure 359.

Lab2: Interactive Control

Let's extend Lab1 to understand how we can add a few dynamically changing effects to our system design by using a TkSlider component from the Interactive Controls and Displays library.

1. Do the following:
   a. Insert TkPlot again (if deleted in earlier lab) or reactivate it (if deactivated earlier)
   b. Insert IID_Uniform noise source from Numeric Sources library
   c. Insert Multiply (Mpy) and Adder (Add) from Numeric Math library
   d. Insert TkSlider from Interactive Controls and Displays library
   e. Modify the DefaultTimeStop = 10 usec for good resolution in the spectrum plot with noise
   f. Connect them as shown below, essentially we are multiplying the IID_Uniform noise amplitude with the TkSlider ranging values of 0.1 (min) to 1 (max) and this will be mixed with our clean SineGen source to introduce Signal + Noise effect for our analysis.

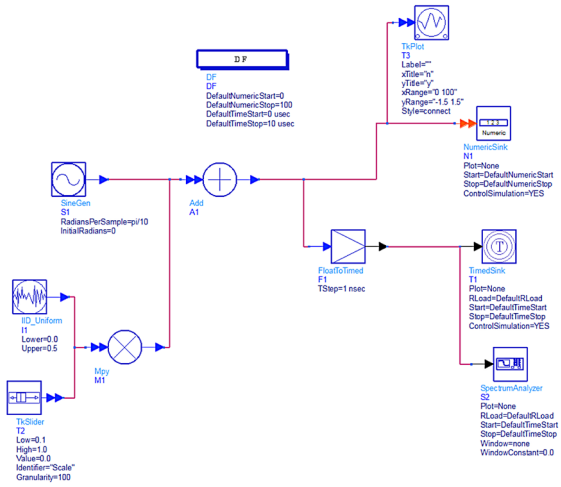


Figure 360.

2. Simulate the design and notice a slider bar with an Identifier shown as Scale (which is the same as in the TkSlider component). When we change the slider, the TkPlot changes in real time....Click Quit once done and observe the data display plot.

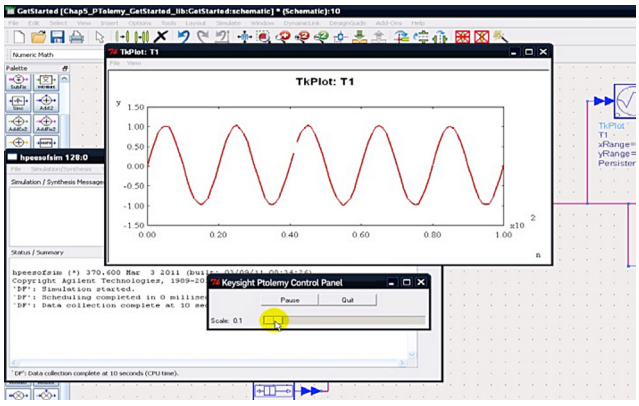


Figure 361.

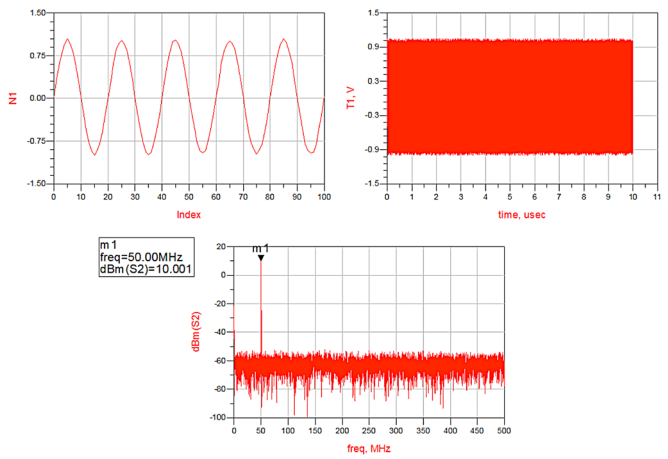


Figure 362.

References

1. J. B. Dennis, *First Version Data Flow Procedure Language*, Technical Memo MAC TM61, May 1975, MIT Laboratory for Computer Science.
2. E.A. Lee and D. G. Messerschmitt, "Static Scheduling of Synchronous Data Flow Programs for Digital Signal Processing," *IEEE Trans. on Computers*, vol. 36, no. 1, pp. 24-35, January 1987.
3. E.A. Lee and D. G. Messerschmitt, "Synchronous Data Flow," Proc. of the IEEE, vol. 75, no. 9, pp. 1235-1245, September 1987.
4. R.M. Karp and R. E. Miller, "Properties of a Model for Parallel Computations: Determinancy, Termination, Queueing," SIAM Journal, vol. 14, pp. 1390-1411, November 1966.

QPSK System Design Using ADS PTolemy

ADS Licenses Used:

– *ADS PTolemy Simulator*

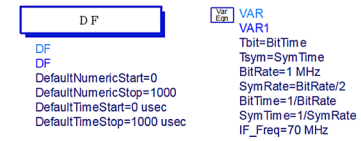
Objective:

With a basic understanding of ADS Ptolemy as described in the chapter Getting Started with ADS Ptolemy, we can now implement a QPSK system to perform end-to-end system simulation and BER analysis to gain more understanding.

Step1: QPSK Modulator Design

1. We will start our system design by building a QPSK modulator network. Create a new workspace with a name **Lab18_QPSK_SystemDesign** and create a new Schematic cell with name **QPSK_Mod**.
2. With the understanding gained from the previous chapter, place the following components on a new schematic:

a. **Bits** source and **change the Type to PRBS** (Notice the stem color is orange indicating this will be a Logic/Integer data type)
b. **Mapper** and make sure ModType=QPSK (this will map the bits to symbol in QPSK format, notice the input stem is orange indicating Integer/Logic and the output is green indicating a complex number for I and Q symbols)
c. **Complex to Rect** converter (CxtoRect) so that we can separate out I and Q symbols.
d. **TkConstellation** from **Interactive Controls and Displays library** to plot constellation. Style in the TkConstellation sink can be kept as **connect** or **dot** depending on whether we want to see constellation points or trajectory.



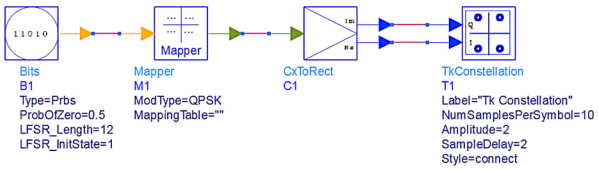


Figure 363.

e. **DF controller** from **Common Components library** and change the NumericStop=1000 and TimeStop=100 usec
f. **VAR block** by clicking on the VAR icon and declare the variables as shown in the graphics
g. Simulate the design and notice the interactive plot as shown below (graphs for both connect and dot options are shown below). These graphs indicate that we are in fact mapping the bits to QPSK format symbols.

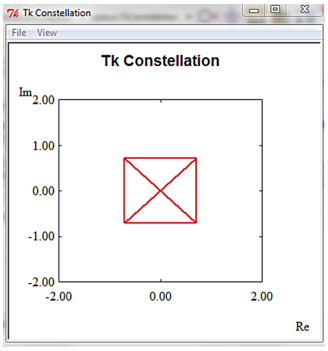


Figure 364.

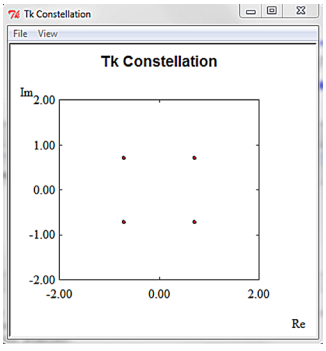


Figure 365.

h. Click on Quit to finish the simulation. We have nothing to plot in data display.

3. Spectrum Shaping (or Band limiting) Filters: Communication systems often employ band limiting or spectrum shaping filters for I and Q channels/signals. Place Raised Cosine filters from Numeric Filters library and define the parameters as shown below in I and Q branches:

   - Interpolation = 8
   - Length = 61
   - Symbol Interval = 8 (should be same as Interpolation)
   - ExcessBW = 0.35 (i.e. 35% excess bandwidth)
   - SquareRoot=YES (this makes it as a Root Raised Cosine Filter)

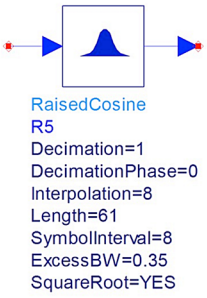


Figure 366.

4. Once finished, the schematic should appear as below (note that we have shifted the TkConstellation sink after the RRC (Root Raised Cosine) filters to see the effect of filter on the constellation.

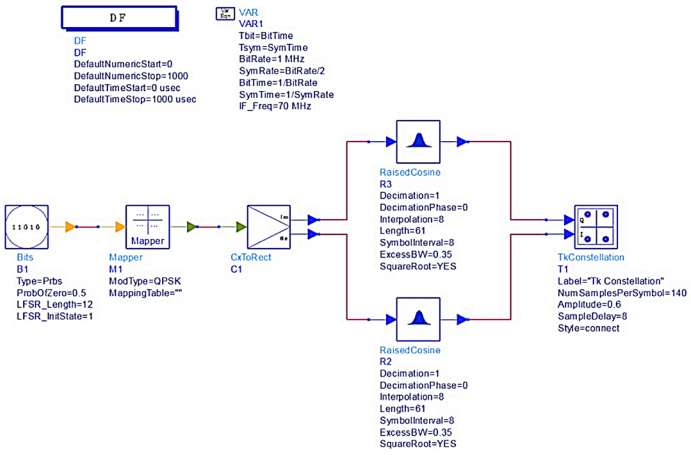


Figure 367.

5. Simulate and observe the constellation after RRC Filters.

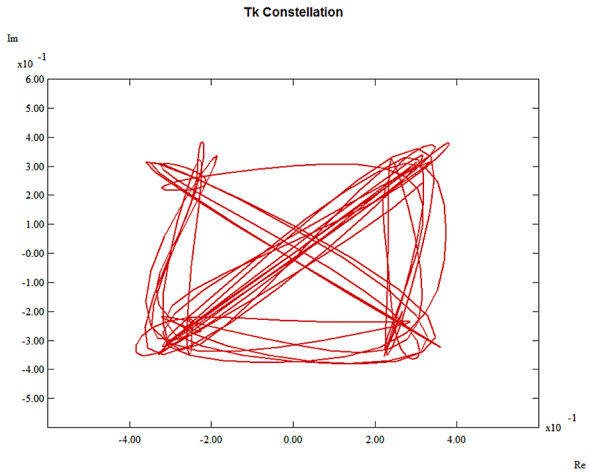


Figure 368.

6. Once we have the band limited I & Q signals, we can perform the IQ modulation, but before that we can view the I & Q spectrum to make sure things are as we desire them to be.
   a. Insert **FloatToTimed** converter and I & Q channels and define **TStep=Tsym/8** (we have interpolated (upsampled) I & Q signal by factor of 8, hence the sampling rate is raise by that amount).
   b. Insert the Spectrum Analyzer sink in the I & Q channel and rename it as I_Spectrum and Q_Spectrum so that we can identify the same while plotting the data graphs.

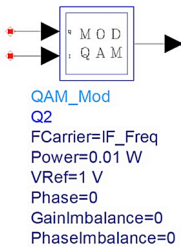


Figure 369.

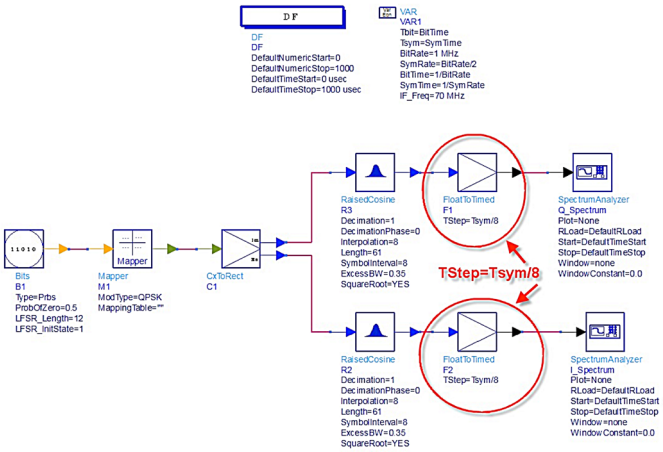


Figure 370.

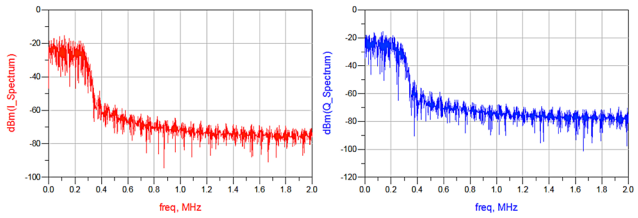


Figure 371.

We can see from the previous graphics that the I & Q spectrum looks to be fine, now we can place a QAM modulator from the Timed Modem library and define the parameters as shown here.

7. Connect the I and Q signals to the respective terminals and place a Spectrum Analyzer sink **(name it "IF_Mod")** to the output of the QAM modulator with a 50-ohm resistor in shunt to make sure we do the power calculations with respect to a 50-ohm reference impedance.
8. Once done, the complete schematic design will look as shown below.
9. Run the Simulation and plot the spectrum of IF_Mod as shown below

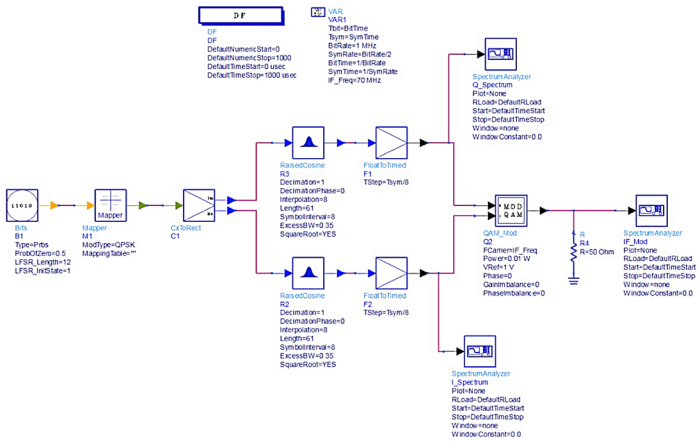


Figure 372.

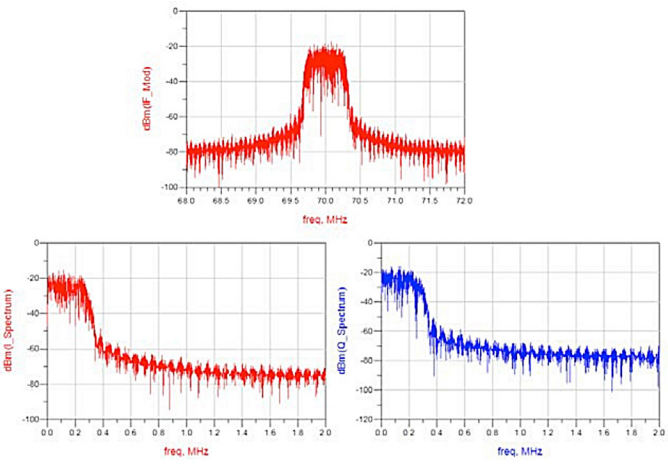


Figure 373.

Step2: Modulated Output Power Calculations

For correct power or voltage calculations, designers need to ensure that the correct load impedance is used in the sinks. By default these sinks use DefaultLoadR, which can be set from the DF Simulation controller's Resistor tab (this will make global changes) or in individual sinks as may be needed as shown below. Another alternate technique is to connect a 50-ohm resistor in parallel to the sinks where voltage or power calculations need to be performed.

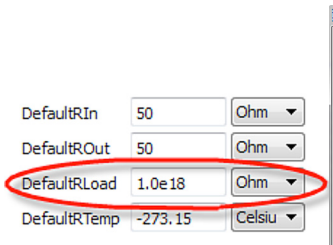


Figure 374.

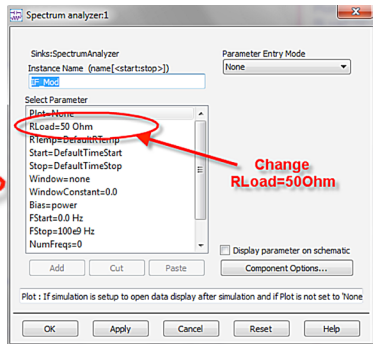


Figure 375.

Change the RLoad to 50 Ohm and change Vref=0.35 and Power to 13 dBm in the modulator as shown below.

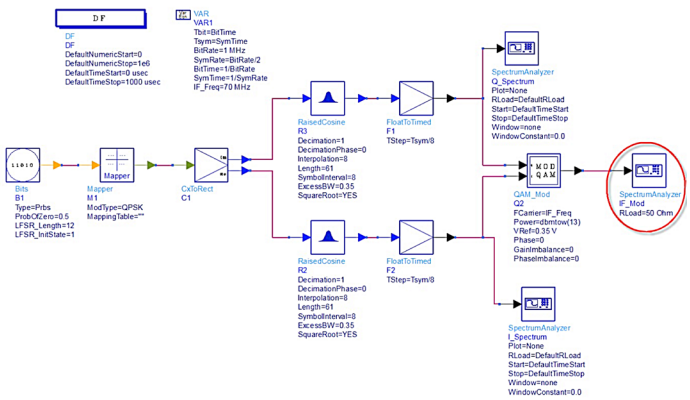


Figure 376.

Double-click on the DF controller, go to Output tab and select IF_Freq, SymRate and click on Add. This allows us to access these variables in the data display to compute power.

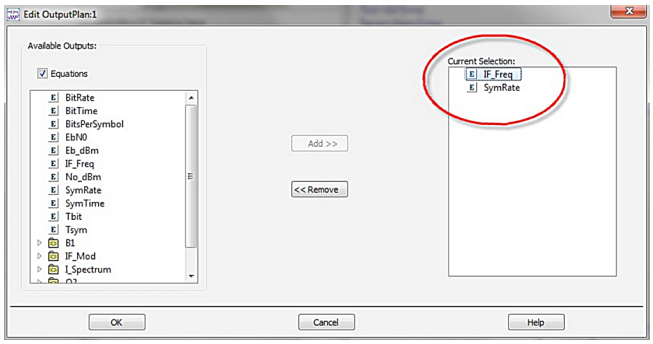


Figure 377.

Run Simulation and use the **Eqn** button on the data display to write an equation to compute Main Channel Power at the Modulator output:

Channel_Power_dBm=spec_power(dBm(IF_Mod),IF_Freq-SymRate,IF_Freq+SymRate)

> ***Note**: spec_power() is the function provided in ADS for Spectral Power calculations and IF_Mod is the name given to the Spectrum Analyzer sink connected at the modulator output. You can use whatever name you might have provided.*

1. Insert a Table plot and drag it to the desired size and select the Equations under Datasets and Equations as shown here.
2. Select the equation name from the list and click on Add>> to add this measurement on the Table.
3. The Channel Power should be @13 dBm as shown on the snapshot on the next page.

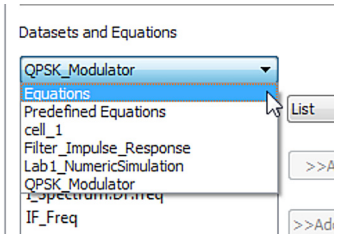


Figure 378.

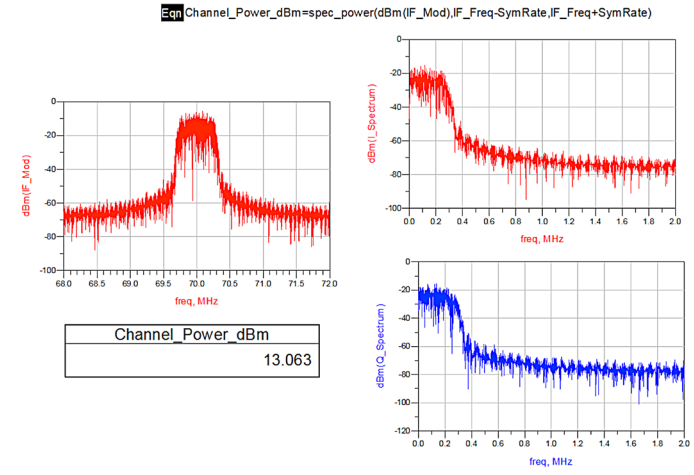


Figure 379.

Step3: QPSK Demodulator and AWGN Channel

After we create the QSPSK modulator design, the remaining sections in our QPSK system is a Demodulator and AWGN (Additive White Gaussian Noise) channel.

1. Copy the earlier created QPSK_Mod cell by the name QPSK_System (*Hint: From the main ADS window right click on the QPSK_Mod cell and select Copy Cell....type the new name in the pop-up window*)
2. Insert a new VAR block and change the Type to Name=Value and enter equations as shown in the snapshot below

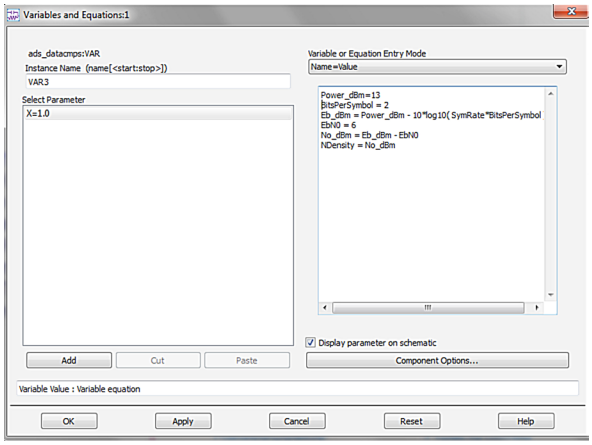


Figure 380.

Equations to be used:

Power_dBm= 13 (Comment: This is the Modulator output power measured previously)

BitsPerSymbol = 2 (Comment: QPSK has 2 bits per symbol)

Eb_dBm = Power_dBm - 10*log10(SymRate*BitsPerSymbol) (Comment: This is to compute the energy per bit)

EbN0 = 6 (Comment: Eb/No variable which will be swept for BER vs. Eb/No curve)

No_dBm = Eb_dBm - EbN0 (Comment: Noise power in dBm to be added to the signal)

NDensity = No_dBm (Comment: Optional variable to read the Noise Power)

3. Insert the following components on the design:
   a. **AddNDensity** (AWGN channel) and define the NDensity as No_dBm or NDesnsity as per the equation variable written earlier)
   b. **QAM_Demod** and define the frequency as IF_Freq
   c. Insert **TimedToFloat** to I & Q channels at the output of QAM Demodulator
   d. Copy/Paste the RRC filters which were used in the Modulator part and change the parameters as follows:
      i. Decimation = 8 (same as Interpolation used earlier)
      ii. Decimation Phase = 3 (we need to choose this parameter carefully to make sure we have a decent constellation at the output of the RRC filters, the range of this parameter is [0-(Decimation – 1)])
      iii. Interpolation = 1
      iv. SymbolInterval = 8 (same as Interpolation which 1)
      v. ExcessBW = 0.35
      vi. Length = 61

e. Connect **TimedSink** at the output of each RRC Filter and name it I_Receive & Q_Receive as applicable.
f. Connect **SpectrumAnalyzer** sink at the output of Noise Channel and name it Demod_Input

4. Double click on the DF controller and go to the Output Tab where you should see SymRate & IF_Freq already added. Select NDensity or No_dBm, EbNo from the list and click on Add button so that these values are available in the data display.

Overall QPSK system schematic should now appear as below

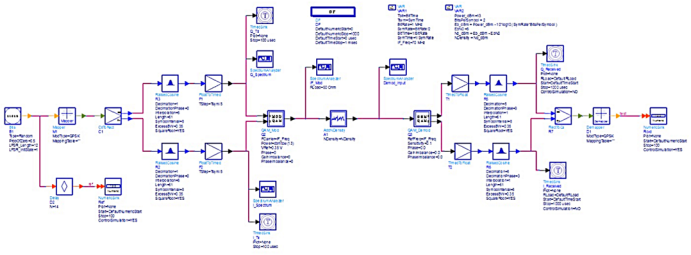


Figure 381.

Run the Simulation and plot a new graph for Demod_Input (which should show the signal plus the noise as per our EbNo value) and a Time Domain graph for received I & Q data. The data display should look as below.

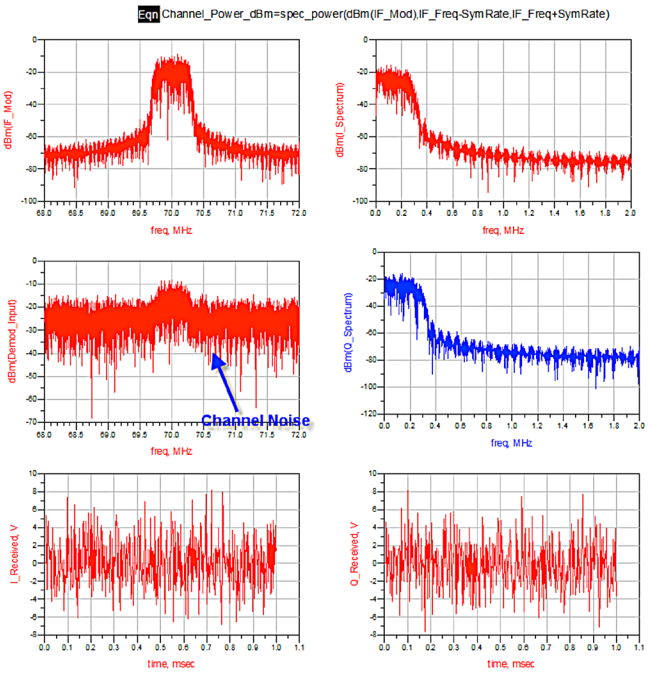


Figure 382.

Step4: BER Simulations

From the steps above, the system seems to be behaving properly and what remains is to perform the BER simulations. Before we simulate BER, we need to synchronize the Tx reference signal (output of Bit source at the input) and the Received Bits (output of the Demapper).

Copy the QPSK_System cell as QPSK_System_BER.

To find the delay, the easiest way is to use the Cross Correlation block in the Numeric-Signal Processing library as shown below.

1. Instead of drawing long wires, we can use the Wire Label 

to name the nodes to be connected, name pin X of the CrossCorr block as “txref” and label the same name at the output of the Bit source at the Input. Name pin Y as “rcvd” and provide the same name label to the output of the Demapper.

2. Connect a Numeric Sink (name it DelayCalc) at the Delay output of the CrossCorr block as shown below to note the delay between the 2 signals (the delay might be shown as negative, which would mean the signal at pin X is delayed with respect to pin Y of the CrossCorr block, usually we should connect ref signal to pin X of the CrossCorr block).

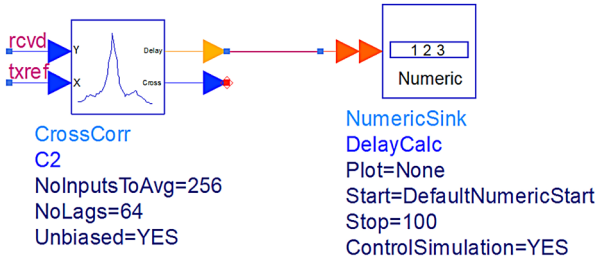


Figure 383.

3. Run the simulation and plot the result of the DelayCalc in a table as shown below:

Index	DelayCalc
0	14.000
1	14.000
2	14.000
3	14.000
4	14.000

Figure 384.

4. These simulation results indicate that the received signal is delayed by 14 samples as compared to the reference signal, and we need to insert a 14-sample delay in the reference signal before we perform BER simulations.
5. Insert a Delay block after the Bit source and modify the Delay value to 14 as we calculated. Label the output of the Delay block as **txref**...

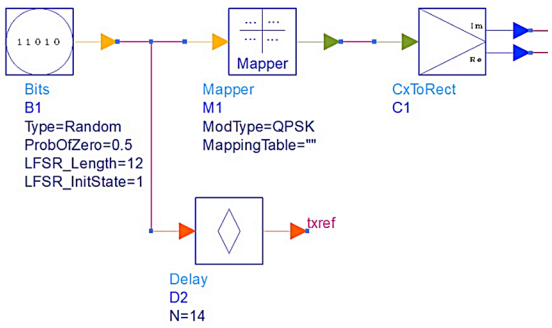


Figure 385.

6. Insert BER_FER sink from Sinks library and set its parameters as shown here:
   a. Start=DefaultNumericStart (it reads start value from PTolemy DF controller)
   b. Stop=DefaultNumericStop (it reads stop value from PTolemy DF controller)
   c. EstRelVariance=0.01 (Confidence factor for BER calculations)

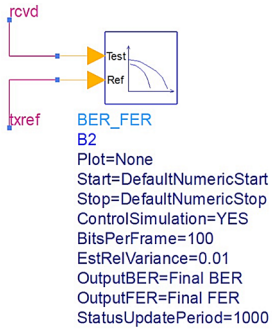


Figure 386.

7. Modify the DF controller to set the values as shown below. Here, we are using 3e6 and may require more for lower BER values as this sink is based on a Monte Carlo technique.

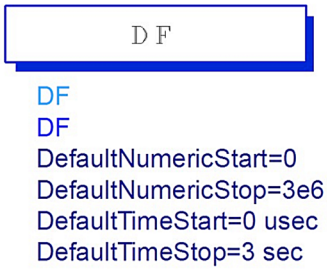


Figure 387.

8. Insert a Parameter Sweep controller from the Controllers library and set its parameters as shown here. This is to provide the sweep to EbN0 from 0 to 10 in a step of 1 which in turn will change the Noise to offer a known EbN0 for specific modulation (QPSK as in our case) for BER calculations.

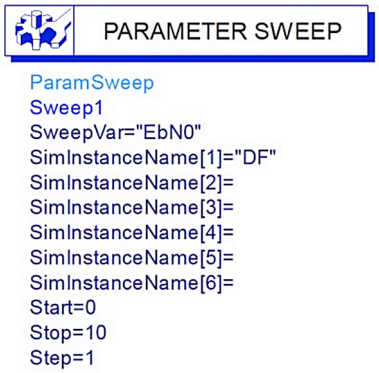


Figure 388.

9. **Disable all other Sinks on the schematic design, otherwise we will get an Out of Memory error due to the huge dataset size because of the large number of samples**.
10. Perform the simulation. Note: it might take a good amount of time on higher EbN0 values as we need a larger number of bits for errors to happen.
11. Once the simulation is finished, insert a rectangular plot in the data display and **select BER from the list of measurements and click on >>Add Vs...>> and select BER. DF.EbN0** (because we want to plot BER vs. EbN0). **Change the Y-axis to be log type** to see proper the Waterfall curve characteristics as shown below.

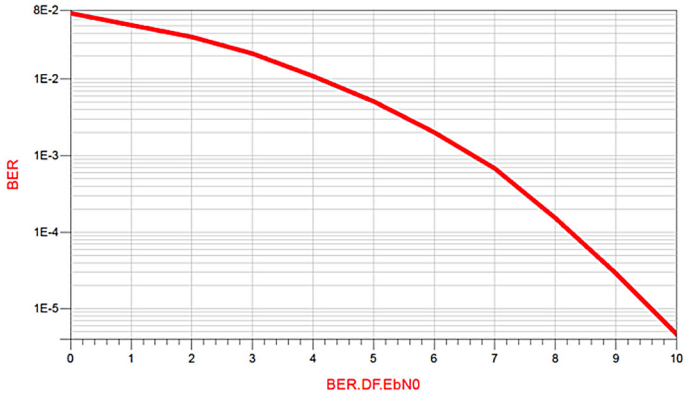


Figure 389.

DSP / RF Co-Simulation Using ADS 2011

ADS Licenses Used:
- ADS PTolemy Simulator
- Circuit Envelope Simulator

Objective:

DSP and RF subsystems often need to be integrated to characterize the complete system performance for various system-level specifications. ADS Ptolemy, which is essentially a mixed signal simulator, offers a way to combine DSP and RF systems together as discussed in this chapter.

DSP RF Co-Simulation Basics

To get started with the Mixed Signal system simulation, we assume that users have a DSP system (as illustrated in Chapter 17) and an RF system (as illustrated in Chapter 5) that are tested independently and found to be working as desired.

For performing an integrated simulation, the following things are to be understood:

a. The RF system will always be called as a sub-circuit on the main DSP design schematic i.e. Ptolemy will be the end-2-end simulator and the RF section will form part of the overall system design schematic.

b. The RF sub-circuit can use either Envelope or Transient as a simulator because only these 2 simulators have time samples, which will essentially allow PTolemy fed input samples to get processed by the RF system/ circuit and then pass the samples back to PTolemy
c. The Source and Sink have to reside in Ptolemy i.e. data should start and end in the Ptolemy environment.
d. If the RF subcircuit is using an Envelope controller, then the RF subcircuit block in Ptolemy should be followed by an EnvOutSelector block in Ptolemy.

Example Case Study:

Let's take a simple example of the QPSK system designed in Chapter 17 and the RF Receiver designed in Chapter 5 to understand this concept of DSP RF co-simulation. The only difference is that we have designed an additional RF Transmitter similar to the RF receiver as illustrated in Chapter 5.

1. Create a new workspace with the name Lab19_RF_DSP_Cosim_wrk
2. Go to DesignKit->Manage Libraries
3. Browse to Lab5_RF_SystemDesign_wrk and select lib.defs under the workspace folder as shown in next snapshot
4. Add lib.defs using the same method for Lab18_QPSK_SystemDesign_wrk

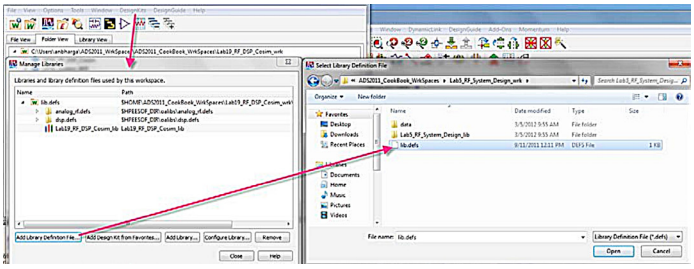


Figure 390.

5. Once the previous workspaces are included, we can see design cells of both of these workspaces in Lab19_RF_DSP_Cosim_wrk as shown below

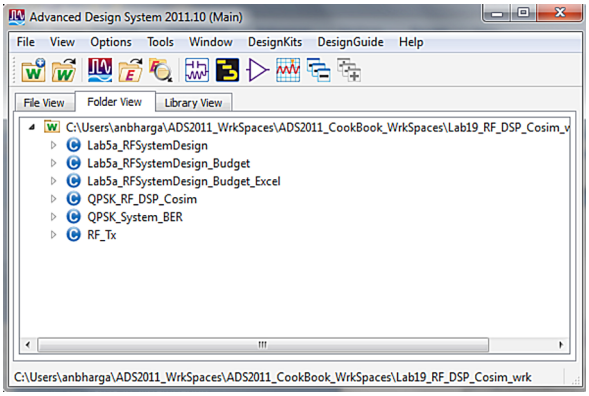


Figure 391.

6. Once these designs are included in our present workspace, we have two options of using them for co-simulation:
   a. **Option 1**: Copy the required cells from these workspaces locally in Lab19 workspace. This will make Lab19 independent of the earlier two workspaces. However, if any changes are done to those designs, then we will need to copy them again for co-simulation.
   b. **Option 2**: Let the original designs remain in their respective workspace and we can just create a cosim schematic in Lab19. However, we need to make sure that paths of the earlier two workspaces don't change; otherwise we need to remove the two lib.defs files and include them with the new path again. The main benefit of this is that if any changes are done to the RF subcircuits or DSP designs, either in the original workspace or while using them in Lab19, they will reflect automatically.
7. We will use Option1 in the present case and copy the required designs into the Lab19 workspace. To do that, right-click on the desired cell and select Copy Cell and select the library in which these cells have to be copied and provide a new name to the copied cell if needed. By default, ADS will add **_v1** in front of the cell name as shown below:

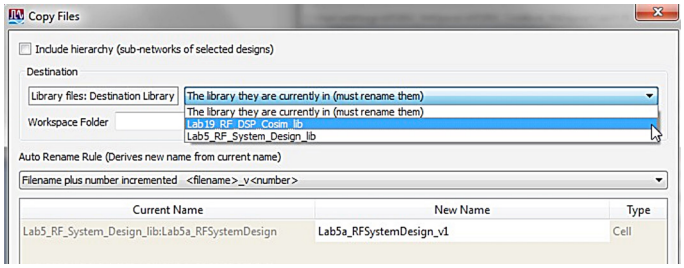


Figure 392.

8. Once all the required designs have been copied to the Lab19 workspace, we can remove the two lib.defs file to avoid any confusion. To remove the lib.defs file, go to **DesignKit->Manage Libraries** and select the name of required lib.defs file and click on **Remove**. Repeat the process for other lib.def file.
9. Now we will be left with two design cells (if the user is following the same nomenclature as mentioned in these chapters):
   a. QPSK_System_BER
   b. Lab5a_RFSystemDesign_v1
10. Create a new Schematic cell with name RF_Tx and create a RF Tx as shown below **(pay special attention to the component specs such as TOI, etc.)**

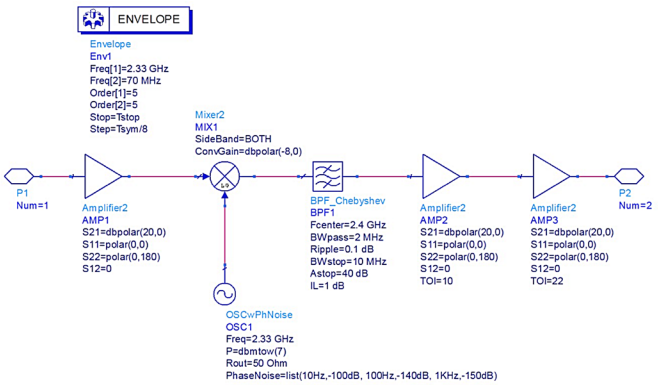


Figure 393.

11. Right-click on Lab5a_RFSystemDesign and select Rename and rename the cell as RF_Rx. Open the same to see the design as shown below (recall that this is the design which was completed during Lab5):

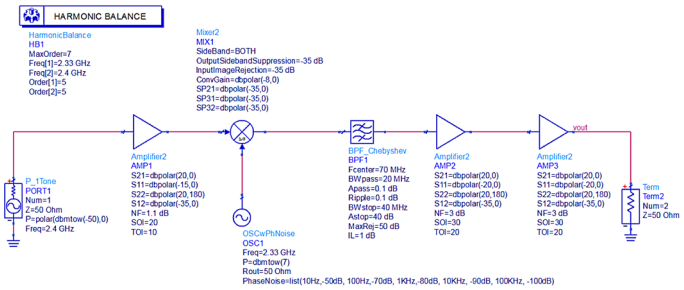


Figure 394.

12. Delete P_1Tone, Term2 and the HB controller from the schematic. Insert a Circuit Envelope controller from the Simulation-Envelope library and set its parameter as shown below. Add Port 1 and Port 2 at the input and output respectively. Once complete, it should look as below:

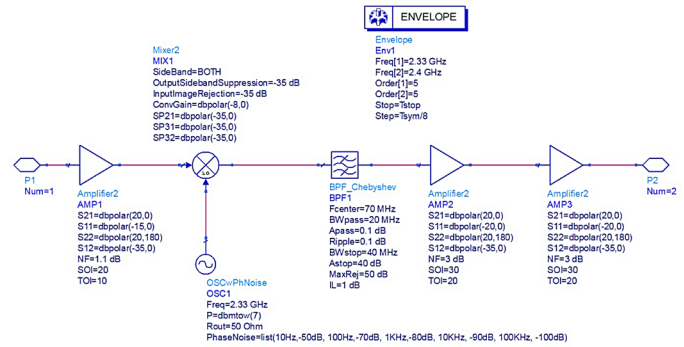


Figure 395. Note: Tsym is already defined in Ptolemy and we will define Tstop later

13. **Open the QPSK_System_BER schematic** and perform following actions:
    a. Disable the BER sink, Delay block (connected to the Ref Bit source) and Parameter Sweep controller.
    b. Enable all Spectrum Analyzer and Timed sinks
    c. Change DefaultNumericStop and DefaultTimeStop to 1000 and 1 msec respectively
    d. Drag and Drop RF_Tx and RF_Rx designs from the main ADS window to this schematic (if you are asked for the Symbol generation method, select Yes and then click OK to auto generate two port symbols)
    e. Place two EnvOutSelector components from the **Circuit Co-simulation** library.
    f. Connect the RF_Tx etc as shown below. Make sure Out Freq in EnvOut selector is defined as per the expected frequency in our system design i.e. for the output of Tx, we defined it to be 2.4 GHz and for the Output of Rx, we have the IF as 70 MHz.
    g. Modify the QAM modulator parameters:
    Power = -30 dBm, Vref=0.7V (this is to feed -30 dBm at the IF port to prevent severe non-linear distortion)

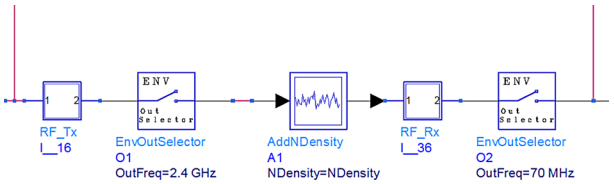


Figure 396.

    h. Change the Spectrum Analyzer connected at the Modulator output to be placed at the Output of EnvOutSelect of RF_Tx so that we can observe the spectrum that got modified by RF Transmitter. Modify the name of this sink to RF_Tx_Spec
    i. Add a variable Tstop = 1 msec (syntax and case should be same as used in the Envelope controller)

14. Perform the simulation and plot two graphs: Tx_RF_spec and Demod_Input as shown below

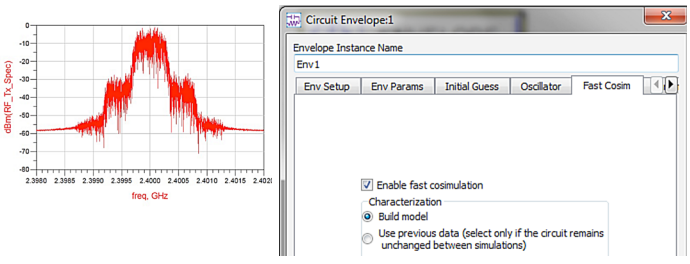


Figure 397. *Notice the shoulders generated at the Tx output due to the Amplifier compression, etc. and also the simulation time taken for this complete system analysis. On a Dual Core Win7 machine, the simulation time reported is ~2 mins. This will make it impractical when we perform BER simulations.*

15. We can use the Fast Cosim option provided in the Envelope controller as long as the RF system/circuits are not changing or getting optimized. Refer to the Fast Cosim documentation for more detail. Go to the RF_Tx subcircuit and double-click on the DF controller->Fast Cosim tab and Select Enable Fast co-simulation as shown here.
16. Go inside RF_Rx and enable the Fast Cosim option, additionally click on **Set Characterization Parameters** and enter Max Input Power = 50 dBm.
17. Come back to the main QPSK system design and run the simulation. Note the simulation time taken with Fast Cosim as shown below....we have a speed improvement of >10x--a huge time savings. The performance comparison snapshot shows the performance is identical when using the Fast Cosim method, hence it can be used for lengthy simulations such as BER later.

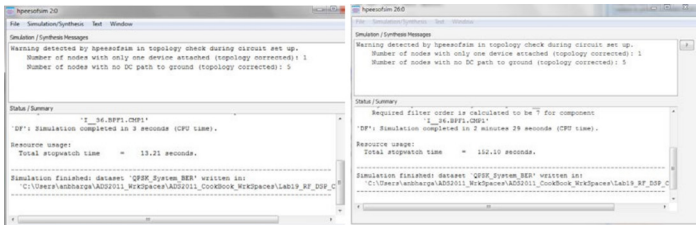


Figure 398. Performance Comparison of System Performance with and without Fast Cosim

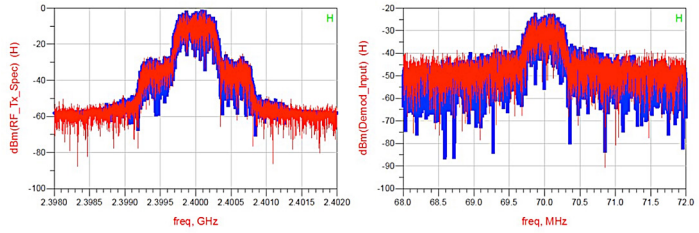


Figure 399.

BER Simulations for RF – DSP Co-simulation:

At this point, we are able to co-simulate RF and DSP designs together and understand various key aspects of the co-simulation. We can extend this idea and now perform BER simulations on the overall system. Do the following:

a. Enable the Delay, BER sinks and Parameter Sweep Controller.
b. Modify the Parameter Sweep to set EbN0 sweep from 0 to 18 in a step of 2.
c. Disable all other sinks as we are going to run a BER simulation, which will involve a large number of samples.
d. Modify the DF controller DefaultNumericStop and DefaultTimeStop to 1e6 and 1 sec respectively (we can use 3e6 and 3 sec also but in this case 1E6 and 1 sec will work fine)
e. The modified schematic should look like the snapshot below:

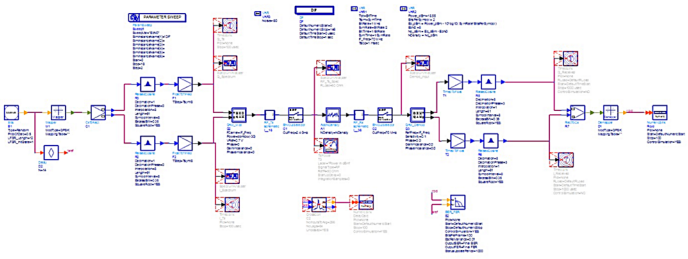


Figure 400.

f. Run the simulation and plot BER vs BER.DF.EbN0 as shown below **(Don't forget to change the Y-axis to log type)**

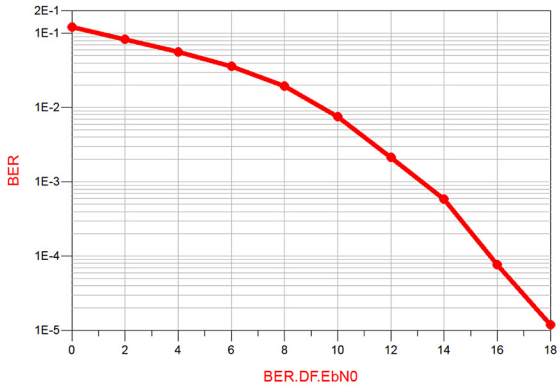


Figure 401.

Appendix

Appendix-A: Antenna Pattern With Circuit Components in ADS 2011

1. From the ADS Main Window, select **Tools->Manage ADS AEL Addons** and select Momentum Circuit Excitation (Beta) as shown below.

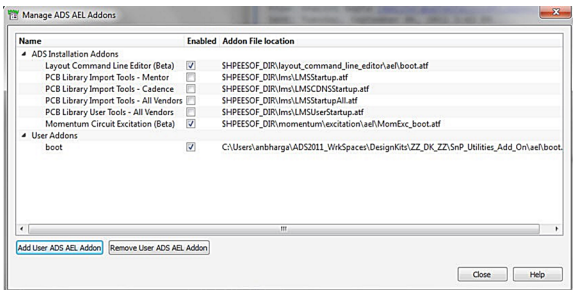


Figure 402.

2. Create a new workspace and create an Antenna design in the layout and set the EM simulation as you normally do by setting up the substrate, simulation frequencies...please take care of adding specific frequency of interest because it may happen that frequency of interest may not appear in the list because of adaptive sweep.

3. In the model/symbol tab of the EM setup.....do the following:
   a. Unselect Include S-Parameter data only
   b. Select Create EM Model when the simulation is launched
   c. Select Create Symbol when the simulation is launched

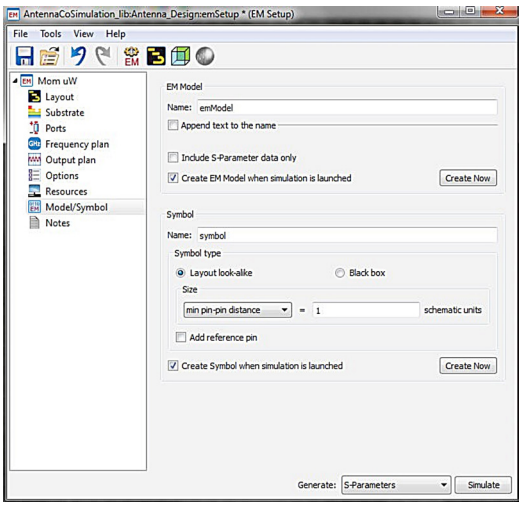


Figure 403.

4. Click on Simulate to run a Momentum simulation and check the S-parameter results.
5. Once the simulation is finished “emmodel” will be created in the cell as shown. Drag and drop it on to a new schematic cell and place the desired active or passive components.

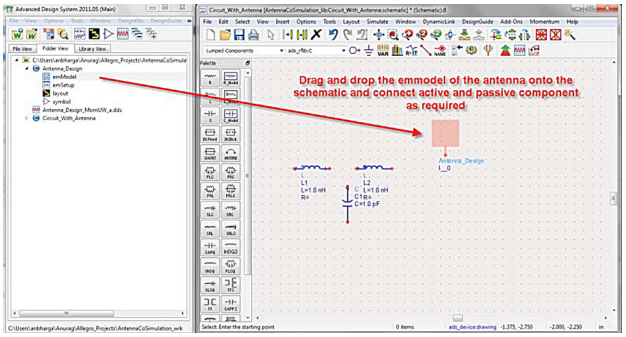


Figure 404.

6. Connect the components and setup the AC or HB simulation as desired (shown below)

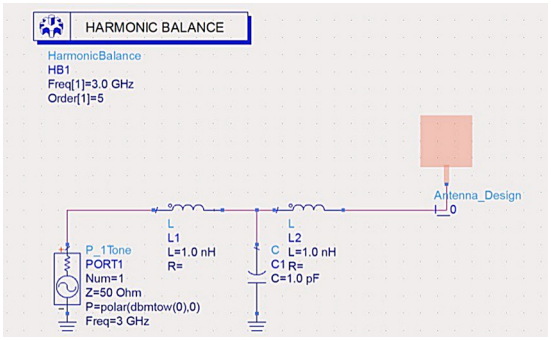


Figure 405.

7. Click on the EM model and click on Choose View for Simulation and select “emmodel” from the list as shown below.

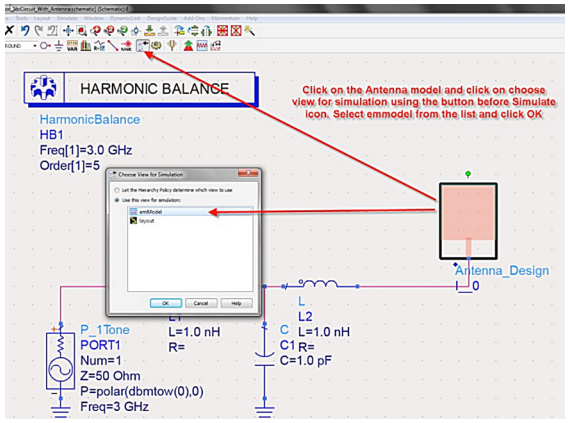


Figure 406.

8. Because we selected Momentum AEL Addon, you should be able to see the Momentum menu on the Schematic. Click on Momentum->Circuit Excitation.

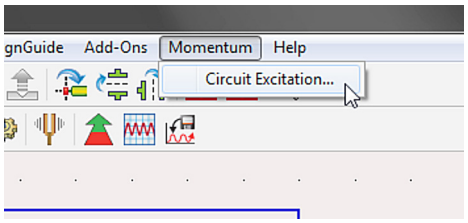


Figure 407.

9. In the pop-up window, click on Run AC/HB Simulation and once it has finished, Visualization fields will be active. Click on Far Field and select the desired frequency from the list and click on Open Visualization.

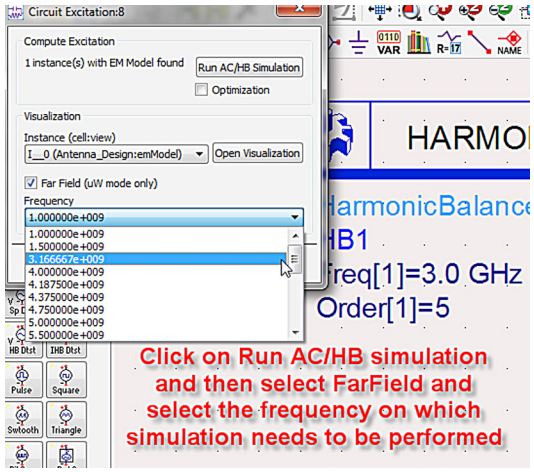


Figure 408.

10. Make note of the message in the pop-up window.

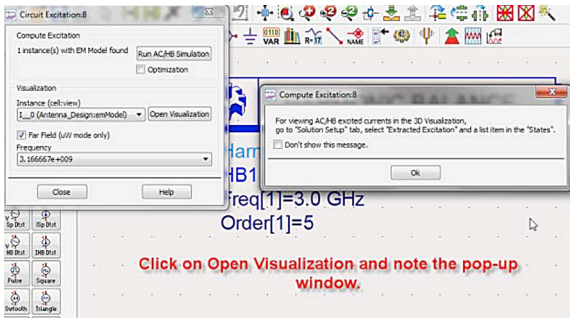


Figure 409.

11. The Far field window will open up...select Extracted Excitation from the Port Setup under the Solution Setup tab as shown below.

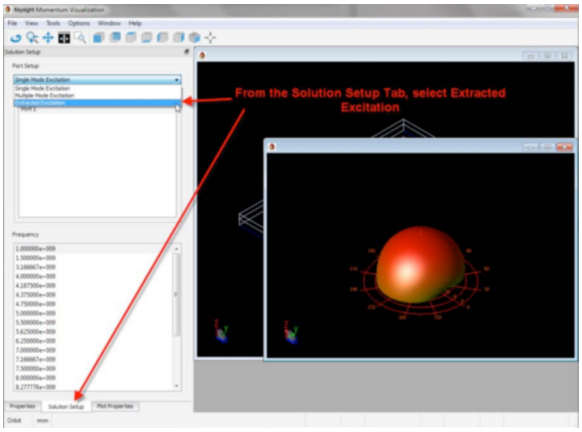


Figure 410.

12. Go to Plot Properties to see various plotting options and to get Antenna Parameter (button) to see various Antenna parameters like Gain, Directivity etc....

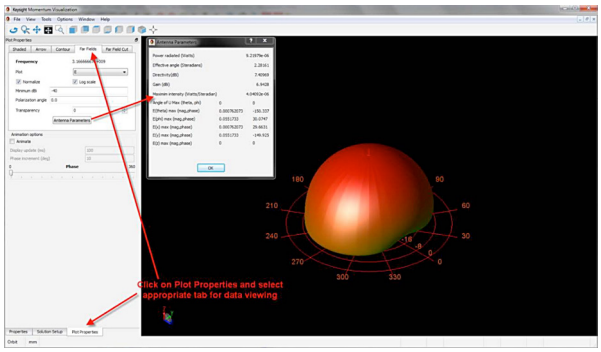


Figure 411.

Appendix-B: How to Perform De-embedding in ADS

Step1:

Prepare the layout 1. e.g. a 20 mm line as shown below. Setup the substrate and setup the simulation conditions such as Edge Mesh, S-parameter start & stop, etc.

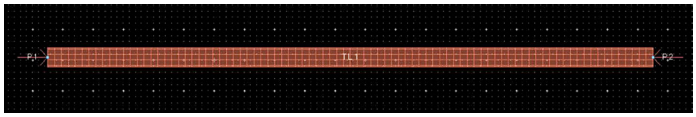


Figure 412.

Step2:

Run a Momentum simulation and observe the data display as shown below.

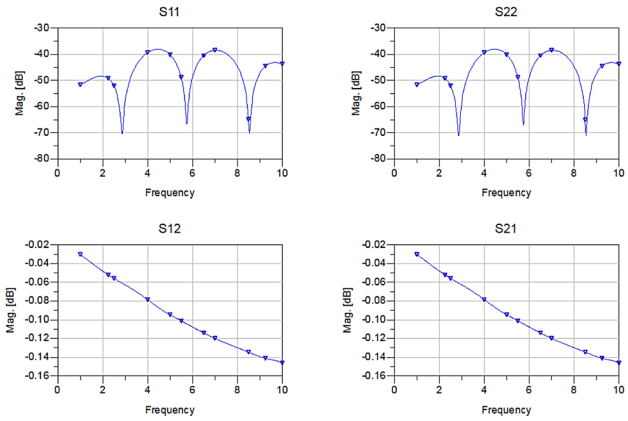


Figure 413.

Step3:

Similarly prepare a 15 mm line layout and use the same substrate and other simulation settings. Run a simulation and observe the data display.

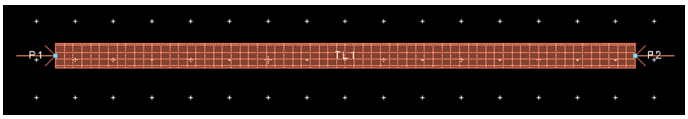


Figure 414.

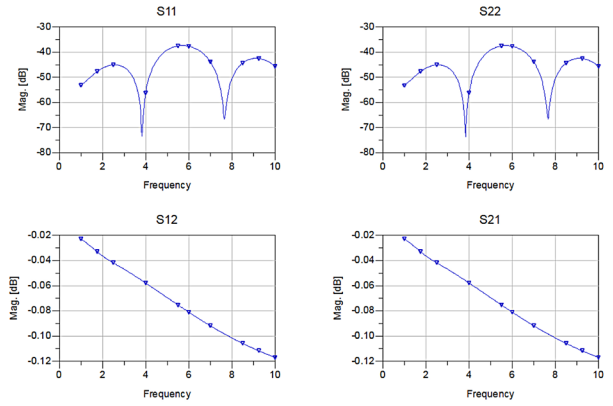


Figure 415.

Step 4:

Prepare the schematic for De-embedding as per the designs. In this case, the original line (20mm) and the line to de-embed (15mm) both have 2 ports, hence we need to place the following components from the Data Items library as shown in next graphics.

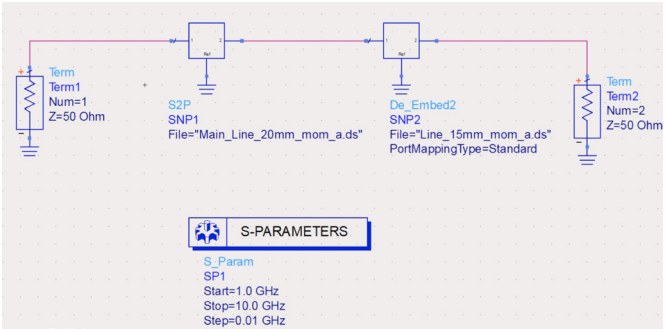


Figure 416.

Double-click on the S2P component and change the File Type = Dataset, browse to the 20 mm Momentum simulation dataset. Similarly, for the 2-port Deembed component, change the File Type=Dataset and browse to the file that needs to be de-embedded (15 mm in this case).

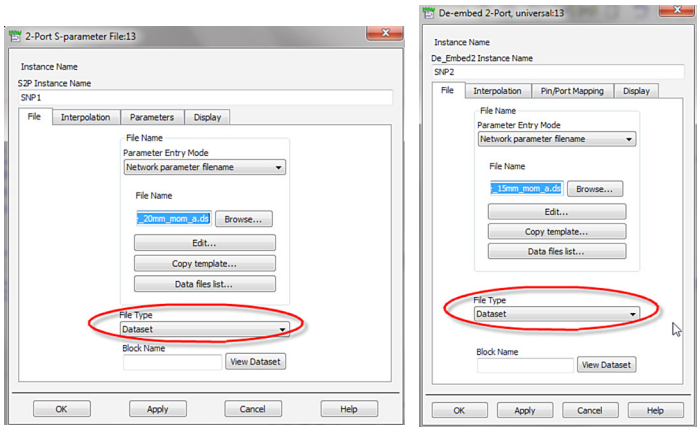


Figure 417.

Setup the S-parameter simulation to see de-embedded results.

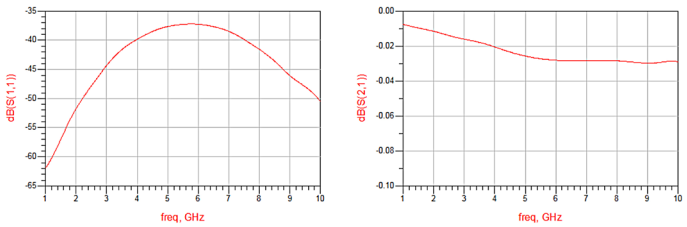


Figure 418.

Verification of the De-embedded Results:

In order to check the results, create a 5 mm line in layout and perform a simulation and compare the Momentum simulation results of the 5 mm line with de-embedded results as shown below.

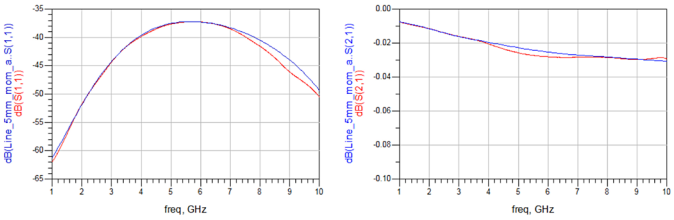


Figure 419.

Appendix-C: How to Use Vendor Component Libraries in ADS 2011

1. ADS 2011 uses a different methodology for Vendor component libraries and sometimes causes confusion to the existing users of ADS who have used earlier ADS releases.
2. All vendor libraries that were present by default in earlier ADS releases are now provided in a zipped format. It is recommended for designers to unarchive them at a central location (a specific folder).
3. All zipped libraries are located in the <ADS install dir>/oalibs/componentLib folder (e.g, C:\Keysight\ADS2011.05\oalibs\componentLib...please note that ADS2011.05 will be as per the version you may be using), in order to unarchive them, go to the ADS Main Window and select DesignKit->Unzip Design Kit...

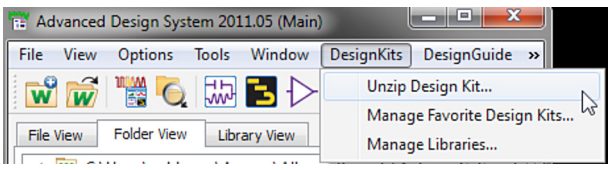


Figure 420.

4. Browse to the location as mentioned above, select the library to unarchive and click on Open. Provide the location/directory where you need to unarchive the library. Repeat the steps for all needed libraries.

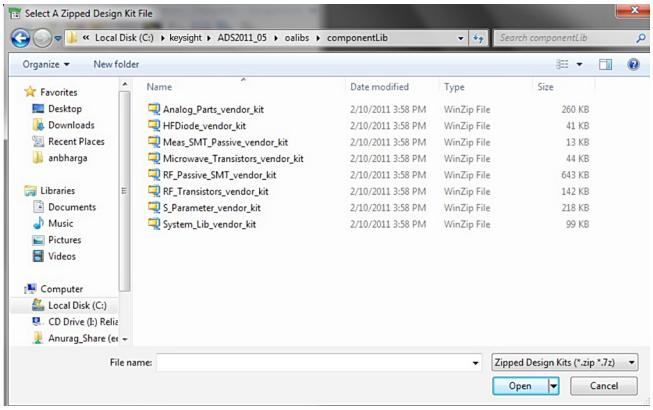


Figure 421.

5. Once done, we can add all these libraries to our favorite list by going to **DesignKit->Manage Favorite Design Kits** as shown below.

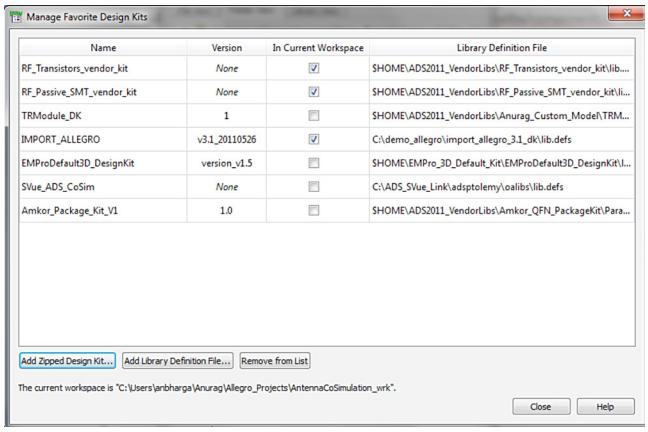


Figure 422.

6. If your desired library does not appear in the list, click on Add Library Definition File and then go to the folder where we have unarchived the library. Each unarchived library folder will have lib.defs file, which is the file we need to point to. We can do this for all needed libraries so that they will appear in the favorite list while we create a new workspace for easy selection as shown below:

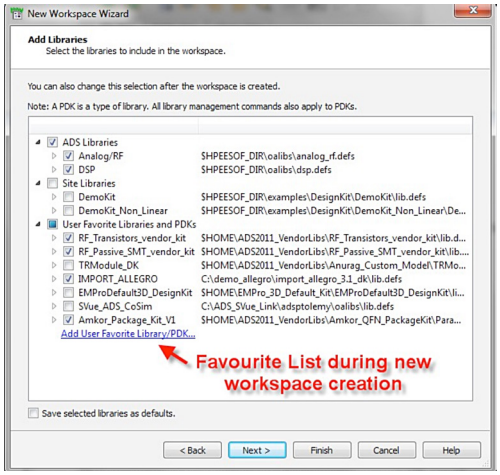


Figure 423.

7. If these libraries are needed on a regular basis, then it will be a good idea to select the option “Save Selected libraries as defaults.” This option will add the currently selected libraries in all the workspaces we create going forward.

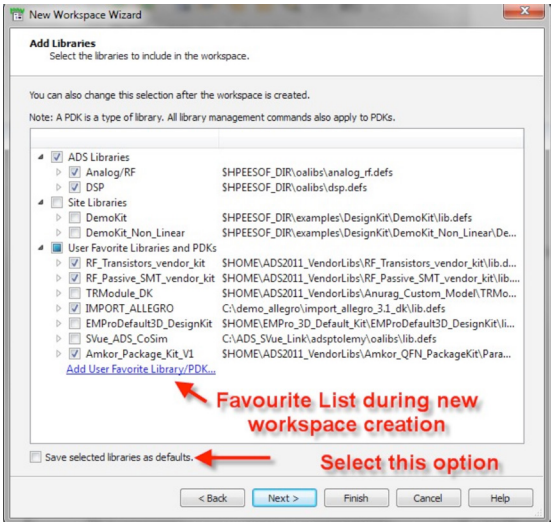


Figure 424.

8. All 3rd party libraries available from various vendor websites like Freescale, Murata, etc. can be added to the favorite list similarly to the process defined above. Please note that each of those libraries will have a lib.defs file after the unzip process.

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Taiwan	0800 047 866
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