High-Speed Digital Industry-Ready Student Certification Program

Introduction

The trend is clear, worldwide demand for data will continue to drive the need for faster networks. Higher baud rates, new modulation formats, and shrinking link budgets will increase the design and test complexities for engineers. Traditional design approaches which rely on open transmitter eyes and a knowledge of the channel loss will no longer ensure adequate link performance. It is critical for engineers entering industry to understand the design and test requirements for next generation high-speed digital links.

Universities must produce industry-ready engineers who are knowledgeable of the tools and processes used in the industry today. This program provides a collaboration between industry and universities to produce and recognize industry-ready engineers. Students completing qualification as Keysight Technologies High-Speed Digital Industry-Ready students have demonstrated immediate value to prospective employers and confirm each university's interest in preparing students for future industry contribution.

A key component of this certification program is the use of Keysight's High-Speed Digital workflow environment, a comprehensive way to simulate, measure, and analyze communications components and systems. The foundations are Keysight's electronic design automation (EDA) software with industry proven design tools along with high-speed digital measurement instruments. Bringing real-world test and measurement earlier into the design process enables design flaws to be captured early and corrected in a time- and cost-efficient manner, reducing overall development cost and improving design-to-manufacturing cycle time.

Level of Experience

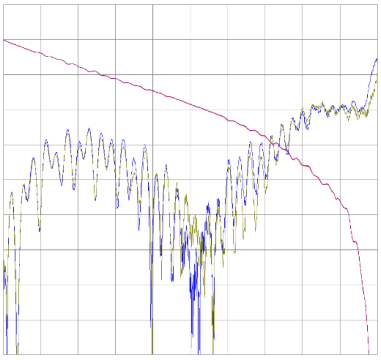
Level 1 certification ensures that the student has completed a signal integrity or high-speed digital design class. Advanced level 2 certification requires hands-on instrument labs and experience correlating measurement results to simulations. The topics covered as part of High-Speed Digital certification offers students insight on how the transmitter, channel, and receiver design impact the overall link performance. Keysight EDA software topics provide students with a knowledge of transmission lines, S-parameters, channel simulation, transient simulation, pulse response, EM models, cross talk, link analysis, and power integrity. For measurement expertise, students will have completed measurement tasks using Keysight vector network analyzers (VNA), data generators, and oscilloscopes. The VNA measurements include single ended and differential transmission line fundamentals, measurements of cables, printed circuit boards, interconnects, along with time and frequency domain comparisons. In addition, as part of the data generator and oscilloscope training, the student will have completed labs demonstrating their understanding of eye diagram measurements, jitter decomposition, and techniques for compensating for channel loss.

(A full list of criteria is included at the end of this document.)

KEYSIGHT PATHWAVE

Keysight Requirements for Universities

- The university must use one or more of Keysight's EDA tools in their curriculum, such as PathWave Advanced Design System (ADS), PathWave RF Synthesis (Genesys), PathWave System Design (SystemVue), and PathWave EM Design (EMPro). The EDA software should be an essential component of the curriculum.
- The university must use Keysight instrumentation for the measurement of their high-speed digital devices (RF vector network analyzer, data generator, oscilloscopes, etc.). These instruments should be an essential component of the lab exercises for advanced level 2 certification.
- The ideal curriculum and lab will involve design, building, measurement, and analysis of high-speed digital components to help students gain real-world understanding of high-speed digital design and measurement techniques.



Qualification Process for Universities and Students

- University completes and submits Keysight High-Speed Digital Industry-Ready Student Certification Program submission form. Additional classroom curriculum and lab material may be required for review by Keysight.
- Keysight certifies that the university course and lab topics meets the program requirements.
- Keysight notifies university of acceptance.
- Students are notified of certification program by the course professor.
- At the end of the course/labs, the Top 15% - 20% of students are eligible for certification.
- Class professor provides Keysight with names of students qualifying for certification based on class grade and quality of lab work.

Student Recognition

- Keysight provides verification of certification with certificate.
- Keysight inserts student name into list on Keysight's website: University Student Certification Program | Keysight
- Keysight's EDA Software team will promote industry recognition of this program.
- Certified students will receive a digital badge that could be used to showcase their HSD competencies.

Levels of certification

There will be two levels of certification. Both levels require satisfactory course completion of a Keysight certified course and/or lab that demonstrate a minimum coverage of software design and instrument measurement topics. One or more classes or labs may be required to satisfactorily complete the required topics.

Certification	Description	Example
Level 1	Basic Keysight EDA tool knowledge for signal integrity. No instruments are required for Level 1 certification. Offline instruments such as a vector network analyzer and oscilloscopes are included with the Keysight EDA bundle.	Transmission line design, channel, and transient simulations. Vector network analyzer S-parameter measurements and TDR/TDT analysis, along with basic eye diagram measurements. Offline instruments can be used for Level 1
Level 2	Additional design analysis with Keysight EDA software and other design tool expertise such as PathWave EM Design (EMPro) or PathWave System Design (SystemVue). Additionally, hands on measurement expertise using Keysight vector network analyzers and oscilloscopes is required.	EM modeling, serial and parallel link analysis, along with power integrity simulations. Hands-on transmission line and channel measurements using vector network analyzer. Hands-on advanced eye diagram measurements including jitter decomposition and techniques for compensating channel loss using oscilloscope.

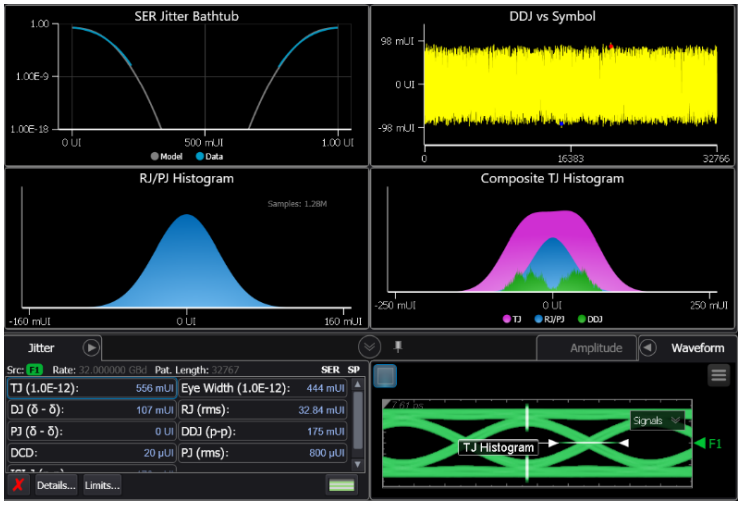
Typical course description

High speed digital design, simulation, and measurements

This laboratory is designed to introduce the electrical engineering students to the design, fabrication and testing of active digital communication links. The core building blocks for a digital link (transmitter, channel, and receiver) are introduced in the simulation and measurement labs. Link impairments such as transmission line losses, reflections, and cross talk are simulated while the impact on actual link performance is measured. Computer Aided Design tools and computer data acquisition strategies are examined in greater detail.

Course topics

- Transmission line design
- Frequency and time domain concepts
- Channel simulation
- Vector Network Analyzer Measurements
- Transmitter (Tx) characterization
- Clock recovery
- Eye diagram measurements
- Jitter decomposition and measurement
- Receiver (Rx) characterization
- Tx and Rx equalization



Keysight EDA software requirements

At least 16 hours of lab usage of Keysight EDA software (ADS, Genesys, SystemVue, or EMPro). Demonstrated knowledge and hands–on experience in the following area listed below. The first 3 topics shown are required for level 1 certification. For level 2 certification, 2 of the topics listed as level 2 must be covered in the curriculum or lab. Substitutions can be made with prior written approval from Keysight Technologies. For example, topics 1 and 2 with topic 5 may be substituted for level 1 certification. Level 2 certification requires level 1 certification (or a course covering equivalent material).

Lab usage	Level	Typical lab	Topics
Using the Workspace Understanding the workspace structure, libraries, schematics, simulation setup and tuning. Learn the steps required for using PathWave Advanced Design System (ADS).	1	**Transmission line design**	• Create a workspace and schematic • Build a differential T-line structure • Set up the S-parameter simulation • Plot the data • • Tune the T-line impedance with trace width and gap

Lab usage	Level	Typical lab	Topics
Using Linear Simulation Tools Channel Simulation.	**1**	**10 Gbps Tx and Rx plus T-Line Channel**	• Build a lossy 10 inch T-Line with a stub and one with a series Z discontinuity. • Use Tx and Rx and FlexDCA EyeProbe • Create Eye Mask and Measure Eye Height and Width • Demonstrate CTLE, FFE, and DFE channel improvements • Parameter Sweep of the Data Rate • Use AMI model for Tx and Rx, sweep corners min, max, typical • 3 Differential Pairs for Crosstalk with Victim and two aggressors
Transient Simulator Transient simulation, system components, and equations.	**1**	**Transient Simulator**	• VtPRBS source with CILD Line Type and VIA Designer for 3 in microstrip to 3 in stripline based on FR4 Stackup • Single Pulse Response with Equalization Cursor Diagram • Compare PRBS spectrum with Single Pulse • Step edge TDR of channel to identify via location and measure excess parasitic L and/or C • Demonstrate Measurement Equation in schematic for calculating impedance • Sweep Risetime from 5% to 50% to show impact on impedance discontinuities • Data display show slider bar to switch data sets for different risetimes • Measured Voltage vs. time waveform source for the channel • Compare S-Parameter iFFT TDR/TDT and Transient Step TDR/TDT for channel length and via parasitics
EM Model of an SI Channel .	**2**	**EM Model of an SI Channel**	• Import ODB++ into new library, explore layer technology • Modify Stack-up for copper above/below core and into prepreg • Simulate 12 port, 3 differential pair, channel • Use SIPro S-parameter viewer to analyzer the EM model in time and frequency domain for single ended and differential performance • Generate subcircuit EM model from SIPro and use in a Channel simulation • EM simulate in SIPro an SI Channel with series components in the path (DC block or resistor termination)
SERDES Digital Standards with IBIS AMI	**2**	**SERDES Digital Standards with IBIS AMI**	• Use IBIS model with NRZ stimulus on the TX and RX to simulate a PCIe differential channel with CILD • Use IBIS model with NRZ stimulus on the TX, Xtalk and RX to simulate an EM extracted model of three PCIe differential channels • Use IBIS model with PAM4 stimulus on the TX, Xtalk and RX to simulate an EM extracted model of three PCIe differential channels • Use IBIS-AMI model with PAM4 and NRZ stimulus and perform CTLE from PCIe standards • Use IBIS-AMI model with PAM4 and NRZ stimulus and perform CTLE from PCIe standards, FFE and DFE
DDR Parallel Bus Digital Standards with IBIS and Bus Simulators.	**2**	**DDR Parallel Bus Digital Standards with IBIS and Bus Simulators**	• Use SIPro to setup and run a DDR simulation with 8 DQ lines by using the DDR setup • Use SIPro to simulate DQ lines and DQS lines while including any components in the simulation • Generate Subcircuit from SIPro simulation and use it in a Memory • Designer Schematic with Controller and Memory Devices
Power Integrity	**2**	**Power Integrity**	• Create a simple PI Schematic with R-L model for the VRM, 5 decoupling caps. Simulate with transient step and AC sweep current loads • Calculate Target Z and the required decoupling C for flat impedance in the frequency domain • Use an optimizer to create a capacitor measure based model (lumped RLC) that matches with the measured S-parameter for a ceramic cap. • Import a PCB with Point of Load power supplies for digital components and run a PIPro DC IR drop with and without sense lines • Duplicate the PIPro DC IR drop to PIPro DC Electric-Thermal and examine the temerature map • EM simulate the PCB Power Distribution Network using PIPro AC and plot impedance at each sink • Turn capacitors on and off to calculate optimum C for PDN inductance, add additional Capacitor models and then run a decap optimization. • • Export PCB PDN EM model with capacitors optimized for flat impedance and connect to VRM state space model and package die load. Run HB, and AC for small and large signal responses.

Keysight instrument measurement requirements

Demonstrated knowledge and hands-on measurement experience with the following topics. Level 1 certification requires offline instruments, VNA (or Physical Layer Test Solution – PLTS) and oscilloscope, which are included in the EDA simulations. For level 2 certification, the student must complete at least (6) lab experiments specifically using instrumentation to reinforce the topics below with hands on measurements. In addition, at least (2) lab experiments that utilize both the Keysight EDA software and instrumentation tools as part of the lab.

Channel Test: RF Vector Network Analyzer Basic Concepts	
Concept of Gain and Loss	
Concept of Electrical Delay	
Understanding Phase	
S-parameters	
Channel Test: RF Vector Network Analyzer Operation Basics	
Systematic error correction on a network analyzer	
1-Port Calibration	• 1-port reflection calibrations • 1-port error model
2-Port Calibration	• full 2-Port SOLT • 2-port error model
Electronic Calibration Kit	
Channel Test: 2 Port Devices – Transmission Line Basic Measurements	
Insertion Loss	
Return Loss	
Group delay measurements	• definition • deviation from linear phase • aperture
Basic filter and attenuator measurements	
Data storage and display	• how to get data out of the analyzer • marker usage • traces, Channels, and Windows
Setting measurement parameters	• IF bandwidth • stimulus settings • averaging
Channel Test: 4 Port Devices – Differential Measurements	
Full 4 Port Calibration - SOLT Calibration	
4 Port Measurements with Coupling - Single Ended Measurements	
Single Ended Port Numbering	
4 Port Measurements with Coupling - Differential Measurements	
Differential Port Numbering	
Differential Transmission Line Characterization	
Channel Test: RF Vector Network Analyzer Advanced Calibration Techniques	
Adapter Characterization	
Frequency Domain De-embedding	

Channel Test: Signal Integrity Analysis – Time and Frequency Domain
VNA Architecture & Block Diagram - narrowband source and receiver w/ directional coupler
TDR/TDT Architecture & Block Diagram - step generator with broadband sampler
Frequency Domain to Time Domain Conversion
Channel Test: Signal Integrity Analysis - Single Ended Time Domain – TDR / TDT
1 Port TDR – Time Domain Reflection (TDR)
Delay Measurements
Impedance Measurements
Impact of Transition Time
2 Port – Time Domain Reflection (TDR) / Time Domain Transmission (TDT)
Time Domain Transmission
Single Ended Frequency Domain / Time Domain
Channel Test: Signal Integrity Analysis – Single Ended Transmission Line Impairments
Loss
Reflections – Impedance Discontinuities
Channel Test: Signal Integrity Analysis – Differential Time Domain – TDR/TDT
4 Port TDR/TDT - 2 Port Differential
Differential Frequency Domain / Time Domain
Channel Test: Signal Integrity Analysis – Differential Transmission Line Impairments
Intra-Line Skew
Mode Conversion
Channel to Channel Crosstalk
Far End Crosstalk (FEXT)
Near End Crosstalk (NEXT)
Channel Test – Signal Integrity Analysis – Interconnect Impairments
Connectors & Cables
Printed Circuit Board & Backplanes
IC Packages
Transmitter Test: Waveform Acquisition - Oscilloscopes
Real Time Oscilloscope Architecture and Block Diagram
Sampling Oscilloscope Architecture and Block Diagram
Triggering Sampling Oscilloscopes
Bandwidth Requirements

Transmitter Test: Clock Recovery
Hardware Clock Recovery - Sampling Oscilloscope
Software Clock Recovery - Real Time Oscilloscope
Jitter Transfer Function (JTF) / Observed Jitter Transfer Function (OJTF)
Transmitter Test: Eye Diagram Analysis
Modulation Formats - NRZ vs. PAM4
Eye Diagram Construction
Eye Diagram Measurements
Single Ended vs. Differential Measurements
Transmitter Test: Jitter and Noise Decomposition
Horizontal / Vertical Eye Closure
Random Jitter / Noise (RJ/RN)
Uncorrelated & Correlated Jitter / Noise
Deterministic Jitter / Noise (DJ/DN)
Data Dependent Jitter / Noise (DDJ/DDN)
Periodic Jitter / Noise (PJ/PN)
Transmitter Testing: Techniques to Compensate for Transmission Impairment
Tx - De-Emphasis / Pre-Distortion
Feed Forward Equalizer (FFE)
Time Domain De-embedding
Rx - Equalization
Feed Forward Equalizer (FFE)
Decision Feedback Equalizer (DFE)
Continuous Time Linear Equalizer (CTLE)
Receiver Test: Bit Error Ratio (BER) Measurements
Bit Error Ratio (BER) Measurement
Instantaneous BER vs. Accumulated BER
BER Insights using an Oscilloscope

Acknowledgement

- Identification as among the best
- Confirmation of technical expertise
- Credentials identified through Keysight webpage and LinkedIn

Added value

- Equipped with industry- ready skills and knowledge
- Creating outstanding resumes
- Increases employment opportunities

Industry access

- Demonstrated value for industry