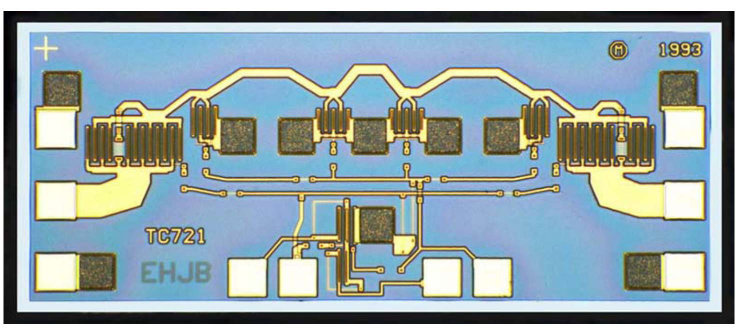
Keysight HMMC-1002
DC–50 GHz Variable Attenuator
1GG7-8001

Data Sheet

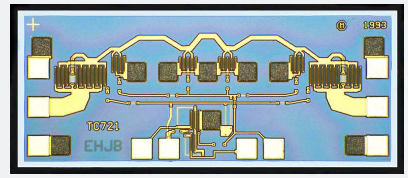


Features

- Specified frequency range: DC to 26.5 GHz
- Return loss: 10 dB
- Minimum attenuation: 2.0 dB
- Maximum attenuation: 30.0 dB

Description

The HMMC-1002 is a monolithic, voltage variable, GaAs IC attenuator that operates from DC to 50 GHz. It is fabricated using WPTC's MMICB process which features an MBE epitaxial layer, backside ground vias, and FET gate lengths of approximately 0.4 µm. The variable resistive elements of the HMMC-1002 are two 750 µm wide series FETs and four 200 µm wide shunt FETs. The distributed topology of the HMMC-1002 minimizes the parasitic effects of its series and shunt FETs, allowing the HMMC-1002 to exhibit a wide dynamic range across its full bandwidth. An on-chip DC reference circuit may be used to maintain optimum VSWR for any attenuation setting or to improve the attenuation versus voltage linearity of the attenuator circuit.



Chip size:
1470 x 610 µm (57.9 x 24.0 mils)
Chip size tolerance:
±10 µm (±0.4 mils)
Chip thickness:
127 ± 15 µm (5.0 ± 0.6 mils)
RF pad dimensions:
60 x 70 µm (2.4 x 2.8 mils) or larger
DC pad dimensions:
75 x 75 µm (3.0 x 3.0 mils) or larger

Absolute Maximum Ratings[1]

Symbol	Parameters/conditions	Minimum	Maximum	Units
V_{DC-RF}	DC voltage to RF ports	–0.6	+1.6	Volts
V_1	V_1 control voltage	–5.0	+0.5	Volts
V_2	V_2 control voltage	–5.0	+0.5	Volts
V_{DC}	DC in/DC out	–0.6	+1.0	Volts
P_{in}	RF input power		17	dBm
T_{mina}	Minimum ambient operating temperature	–55		°C
T_{maxa}	Maximum ambient operating temperature		+125	°C
T_{stg}	Storage temperature	–65	+165	°C
T_{max}	Maximum assembly temperature (for 60 seconds maximum)		+300	°C

1. Operation in excess of any one of these conditions may result in damage to this device

DC Specifications/Physical Properties

(T_A = 25 °C)

Symbol	Parameters/conditions	Minimum	Typical	Maximum	Units
I_{V1}	V_1 control current, (V_1 = –4 V)	5.3	9.3	12	mA
I_{V2}	V_2 control current, (V_2 = –4 V)	5.3	9.3	12	mA
V_p	Pinch-off voltage, (V_2, W/V_1 = 0 V) (Four 200 µm wide shunt FETs, V_{DD} = 1 V @ RF_{in}, I_{DD} = 5 mA)	–0.6	–1.3	–2.5	Volts

Electrical Specifications[1]

(T_A = 25 °C, Z_0 = 50 Ω)

Parameters/conditions	Frequency (GHz)	Minimum	Typical	Maximum	Units
Minimum attenuation, |S21|(V_1 = 0 V, V_2 = –4 V)	1.5		1.0	2.4	dB
	8.0		1.4	2.4	dB
	20.00		1.7	2.4	dB
	26.5		2.0	2.4	dB
	50.0		3.9		dB
Input/output return loss @ minimum attenuation setting, (V_1 = 0 V, V_2 = –4 V)	< 26.5	10	16		dB
	< 50.0		8		dB
Maximum attenuation |S21|(V_1 = –4 V, V_2 = 0 V)	1.5	27	30		dB
	8.0	27	38		dB
	20.0	27	38		dB
	26.5	27	40		dB
	50.0		35		dB
Input/output return loss @ maximum attention setting, (V_1 = –4 V, V_2 = 0 V)	< 26.5	8	10		dB
	< 50.0		10		dB
DC power dissipation, (V_1 = –5 V, V_2 = –5 V) (does not include input signals)				152	mW

1. Attenuation is a positive number; whereas, S_{21} as measured on a network analyzer would be a negative number.

Applications

The HMMC-1002 is designed to be used as a gain control block in an ALC assembly. Because of its wide dynamic range and return loss performance, the HMMC-1002 may also be used as a broadband pulse modulator or single-pole single-throw, non-reflective switch.

Operation

The attenuation value of the HMMC-1002 is adjusted by applying negative voltage to V2. At any attenuation setting, optimum VSWR is obtained by applying negative voltage to V_1. Applying negative voltage (V_2) to the gates of the shunt FETs sets the source-to-drain resistance and establishes the attenuation level. Applying negative voltage (V_1) to the gates of the series FETs optimizes the input and output match for different attenuation settings. In some applications, a single setting of V_1 may provide sufficient input and output match over the desired attenuation range (V_2). For any HMMC-1002 the values of V_1 may be adjusted so that the device attenuation versus voltage is monotonic for both V_1 and V_2; however, this will slightly degrade the input and output return loss.

The attenuation and input/output match of the HMMC-1002 may also be controlled using only a single input voltage by utilizing the on-chip DC reference circuit and the driver circuit shown in Figure 4. This circuit optimizes VSWR for any attenuation setting. Because of process variations, the values of V_{REF}, R_{REF}, and R_L are different for each wafer if optimum performance is required. Typical values for these elements are given. The ratio of the resistors R_1 and R_2 determines the sensitivity of the attenuation versus voltage performance of the attenuator.

Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

The Keysight Technologies, Inc. application note *GaAs MMIC ESD, Die Attach and Bonding Guidelines*, literature number 5991-3484EN, provides basic information on these subjects.

Additional References

2-26.5 Variable Gain Amplifier Using HMMC-5021/22/26 and HMMC-1002 GaAs MMIC Components, Application Note, literature number 5991-3543EN

HMMC-1002 Attenuator: Attenuation Control, Application Note, literature number 5991-3555EN

DC-50 GHz Variable Attenuator: S-Parameters, Application Note, literature number 5991-3556EN

HMMC-1002 DC-50 GHz Variable Attenuator: Switching Speed Limitations, Application Note, literature number 5991-3557EN

HMMC-1002 50 GHz Attenuator 0-50 GHz Performance, Technical Overview, literature number 5991-3554EN

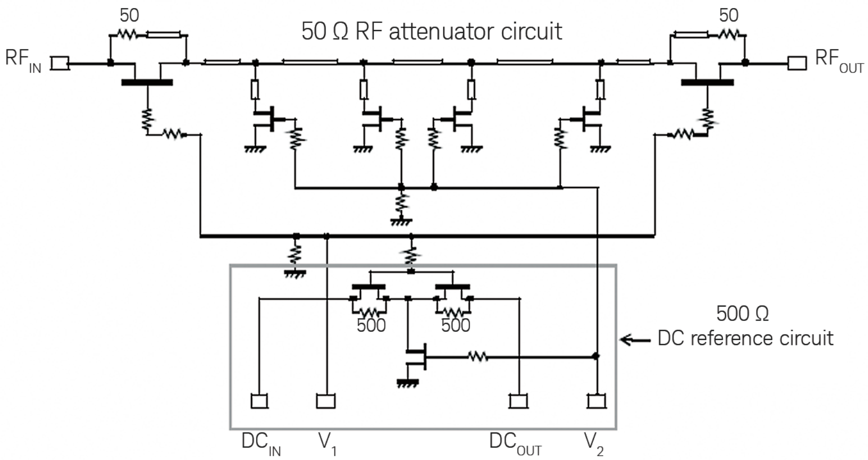


Figure 1. Schematic

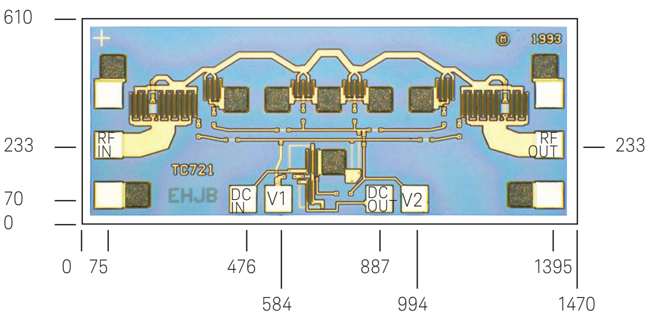


Figure 2. Bonding pad locations

Notes:

1) All dimensions in microns and shown to center of bond pad.
2) DC_{in}, V_1, DC_{out}, and V_2 bonding pads are 75 x 75 microns.
3) RF input and output bonding pads are 60 x 70 microns.
4) Chip thickness: 127 ± 15 µm.

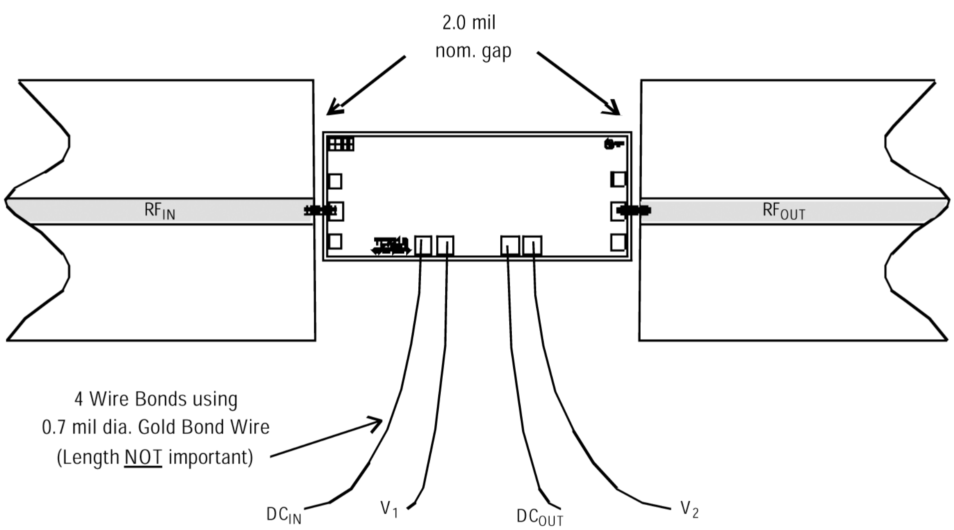


Figure 3. Assembly diagram

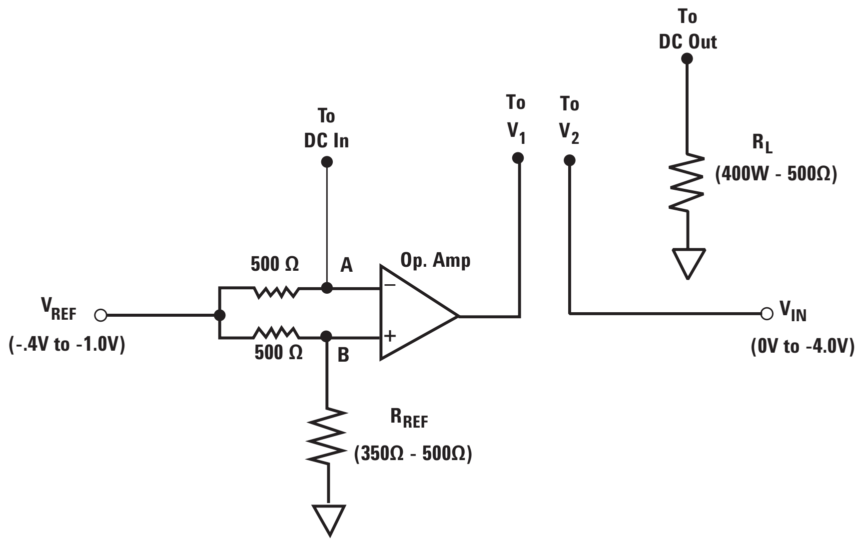


Figure 4. Attenuator driver

Typical Performance

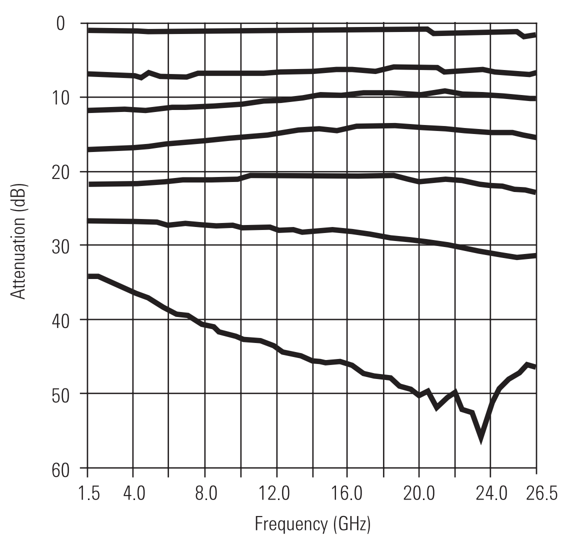


Figure 5. Attenuation vs. frequency[1]

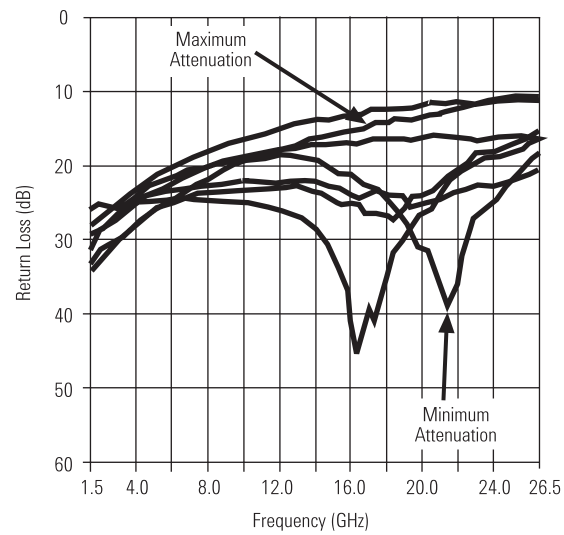


Figure 6. Output return loss vs. frequency[1]

1. Data obtained from on-wafer measurements. T_{chuck} = 25°C.

Typical Power Performance

(NOTE: All attenuation settings were done at 1 GHz)

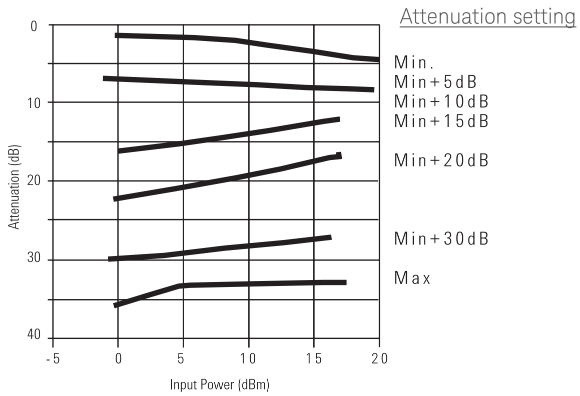


Figure 7. Attenuation vs. input power @ 50.0 MHz[1]

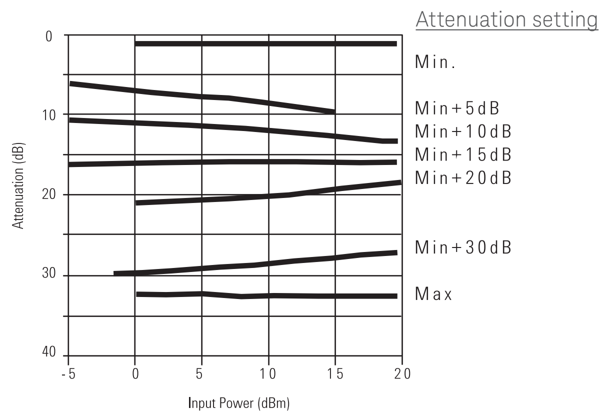


Figure 8. Attenuation vs. input power @ 2.0 GHz[1]

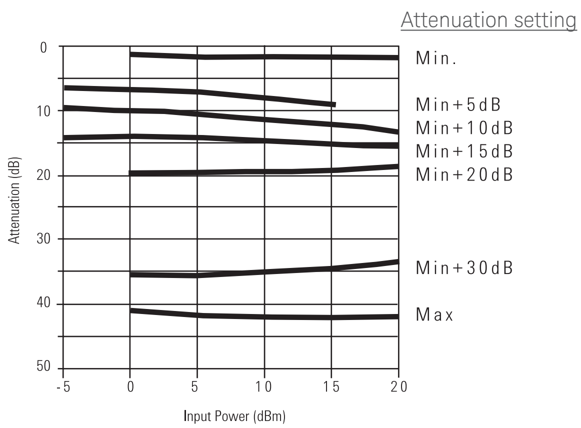


Figure 9. Attenuation vs. input power @ 10.0 GHz[1]

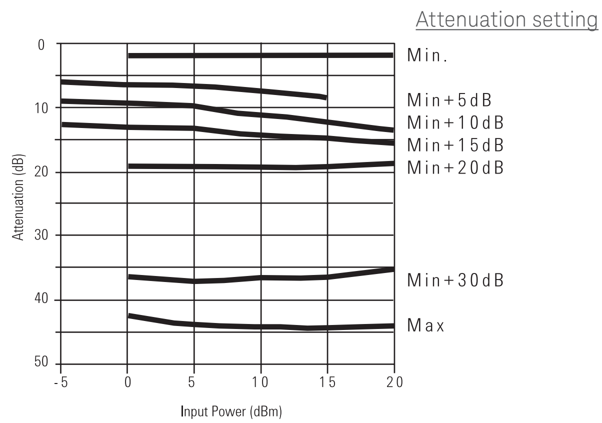


Figure 10. Attenuation vs. input power @ 14.0 GHz[1]

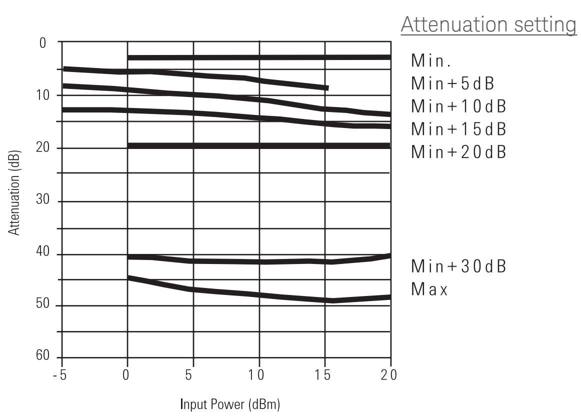


Figure 11. Attenuation vs. input power @ 18.0 GHz[1]

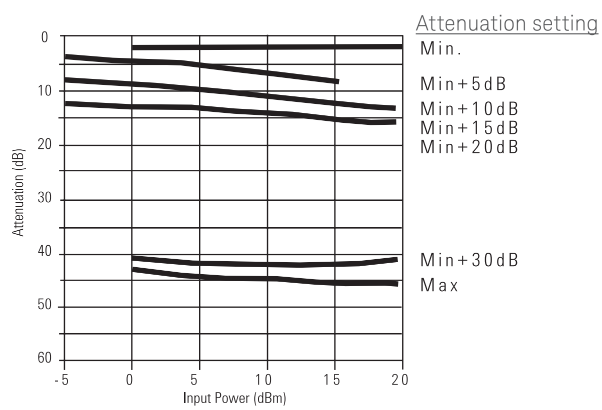


Figure 12. Attenuation vs. input power @ 22.0 GHz[1]

1. Data taken with the device mounted in connectorized package

Typical Harmonic Performance

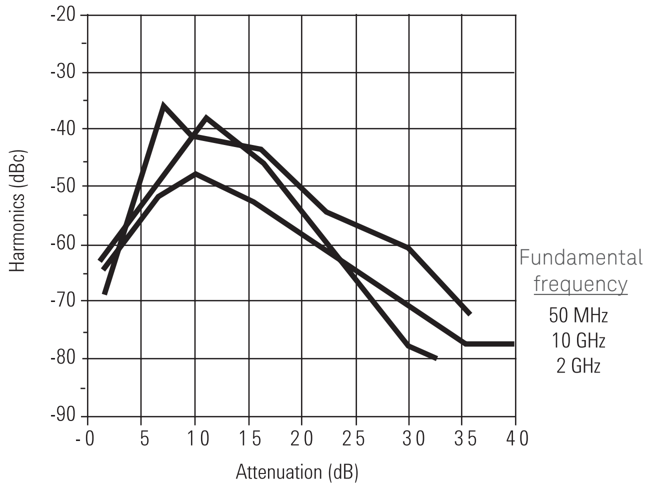


Figure 13. Second harmonic suppression vs. attenuation, input power = 0.0 dBm[1]

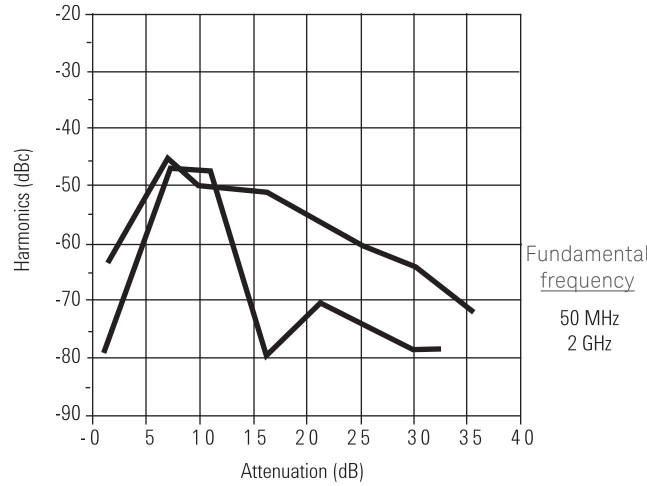


Figure 14. Third harmonic suppression vs. attenuation, input power = 0.0 dBm[1]

1. Data taken with the device mounted in connectorized package

Typical Temperature Performance

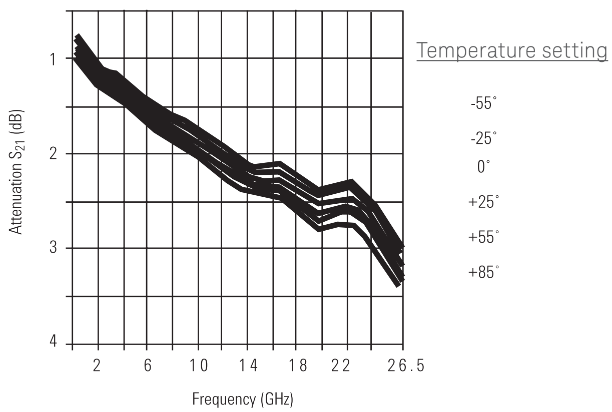


Figure 15. Attenuation vs. temperature @ minimum attenuation[1]

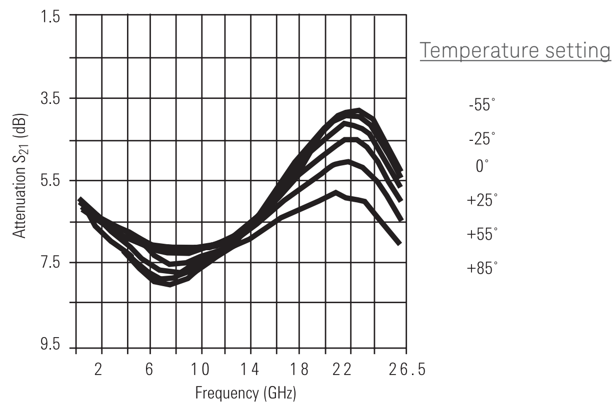


Figure 16. Attenuation vs. temperature @ 5 dB attenuation[1]

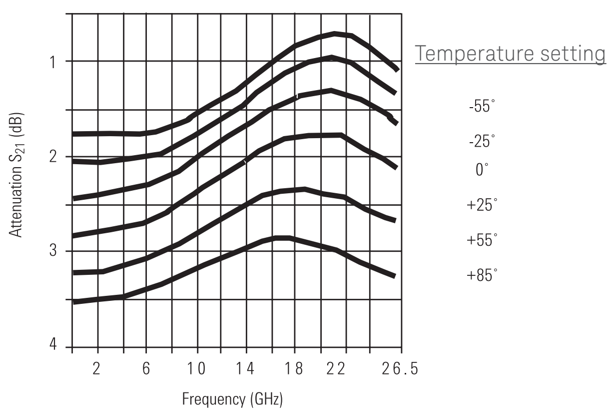


Figure 17. Attenuation vs. temperature @ 10 dB attenuation[1]

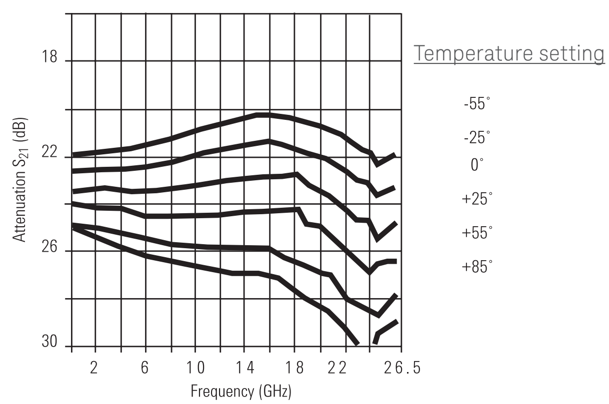


Figure 18. Attenuation vs. temperature @ 20 dB attenuation[1]

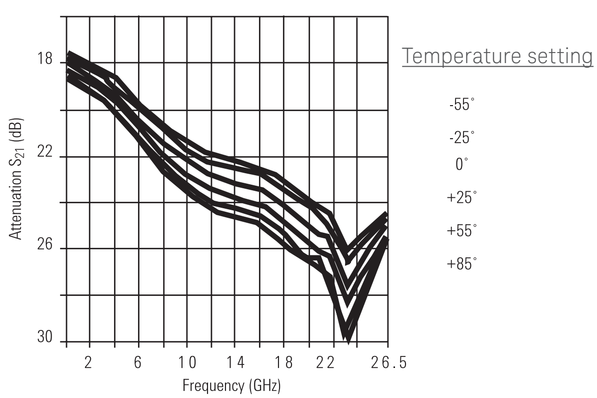


Figure 19. Attenuation vs. temperature @ 30 dB attenuation[1]

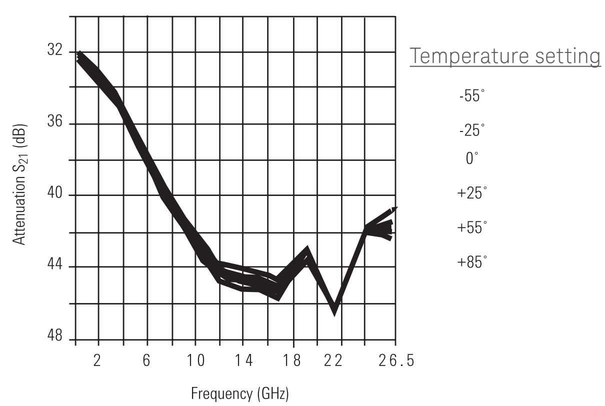


Figure 20. Attenuation vs. temperature @ maximum attenuation[1]

1. Data taken with the device mounted in connectorized package

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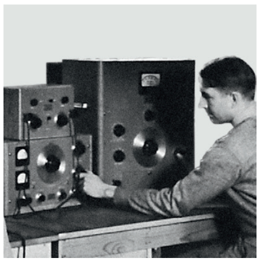
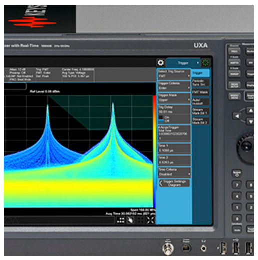


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